6 Publishable Summary

OSIRIS project, a Research and Innovation Action (RIA), aims at improving substantially the cost effectiveness and performance of gallium nitride (GaN) based millimetre wave components. The project proposes to elaborate innovative SiC material using isotopic sources. This material will offer thermal conductivity improvement of 30% which is important for devices dissipating a lot of power, in particular in SiC power electronics and in microwave device using GaN high electron mobility transistors (HEMT) grown on SiC semi-insulating substrates. OSIRIS project will allow reinforcing GaN technology penetration into the market by cost effectiveness of the SiC substrates and circuit performances improvement thanks to better heat spreading close to the dissipative area.

For microwave GaN/SiC HEMT this isotopic approach could create a complete shift in the currently used substrate / GaN epi-wafer technology; it intends to grow high thermal conductivity (+30%) semi-insulating SiC on top of low cost semiconducting SiC substrates (widely used by the power electronics and LED industries). Reduced layer thickness is necessary as only the top 50 to 100µm SiC wafer is really useful as the substrate itself is currently thinned to realise microstrip waveguided microwave circuits.

For power electronics, this isotopic innovation will be essentially focused on thermal improvement, i.e. better electron mobility at a given power dissipation as mobility and drift mobility decrease with temperature and also better carrier transport thanks to lower scattering rates. Schottky and p-i-n diodes will be tested using this material, which however will have to be doped while microwave devices need semi-insulating materials.

The improved thermal SiC properties will be obtained by using single isotopic atoms for silicon and carbon, namely ^{28}Si and ^{12}C. The SiC wafer size will be targeted to 100mm (4-inches) which is today widely used on industry.

It is expected to bring the technology from a TRL of 3 at the project commencement to a TRL of 5 at its achievement.

It is estimated that the 4'' SI SiC substrate price using the innovative "isotopic" approach could be decreased from US $4000 down to about US $2200 thanks to the use of lower cost SiC substrates as handle. The SiC wafer market is expected to grow from $59m in 2013 to $553m in 2020, covering all electronics applications.

Lead by III-V Lab (F), leading European lab in the field of GaN technology, the Consortium includes

- Classic (Sw), which is developing a challenging isotopic SiC approach,
- relying on recent demonstration and long expertise of the University of Linkoping (Sw);
- Isosilicon which will extract the selected carbon and silicon isotopes for the SiC growth;
- NORSTEL (Sw) a leading SiC substrate supplier;
- UMS (F-G) the largest III-V component manufacturer in Europe for microwave applications;
- Ascatron (Sw) involved in SiC technology for power electronics;
- CNRS-CIMAP (F) lab involved in material analysis;
- STUBA (SL), a University with expertise in material and device characterisation;
- Intraspec Technologies (F), a company involved in wafer and device characterisation;
- Infineon (G) will be associated to the OSIRIS project to check the isotopic SiC material for Schottky diodes.

By nature, the Consortium is strongly committed in exploiting the project results.