5. Ethics and Security

5.1 Ethics

Not applicable

5.2 Security[51]

- activities or results raising security issues: NO
- 'EU-classified information' as background or results: NO)

6. Publishable Summary

The SeNaTe project is the next in a chain of thematically connected ENIAC JU KET pilot line projects which are associated with 450mm/300mm development for the 12nm and 10nm technology nodes. The main objective of the project is the demonstration of the 7nm IC technology integration in line with the industry needs and the ITRS roadmap on real devices in the Advanced Patterning Center at imec using innovative device architecture and comprising demonstration of a lithographic platform for EUV and immersion technology, advanced process and holistic metrology platforms, new materials and mask infrastructure.

A lithography scanner will be developed based on EUV technology to achieve the 7nm module patterning specification. Metrology platforms need to be qualified for N7's 1D, 2D and 3D geometries with the appropriate precision and accuracy. For the 7nm technology modules a large number of new materials will need to be introduced. The introduction of these new materials brings challenges for all involved processes and the related equipment set. Next to new deposition processes also the interaction of the involved materials with subsequent etch, clean and planarization steps will be studied. Major European stakeholders in EUV mask development will collaboratively work together on a number of key remaining EUV mask issues.

The first two years of the project will be dedicated to find the best options for patterning, device performance, and integration. In the last year a full N7 integration with electrical measurements will be performed to enable validation of the 7nm process options for High Volume Manufacturing.

The SeNaTe project relates to the ECSEL work program topic Process technologies – More Moore. It addresses and targets as set out in the MASP at the discovery of new Semiconductor Process, Equipment and Materials solutions for advanced CMOS processes that enable the nano-structuring of electronic devices with 7nm resolution in high-volume manufacturing and fast prototyping.

The project touches the core of the continuation of Moore's law and covers all aspects of 7nm process development. The cost aware development process, which is at the core of the project, will

[51] Article 37.1 of Model Grant Agreement. *Before disclosing results of activities raising security issues to a third party (including affiliated entities), a beneficiary must inform the coordinator — which must request written approval from the Commission/Agency;* Article 37. *Activities related to 'classified deliverables' must comply with the 'security requirements' until they are declassified; Action tasks related to classified deliverables may not be subcontracted without prior explicit written approval from the Commission/Agency.; The beneficiaries must inform the coordinator — which must immediately inform the Commission/Agency — of any changes in the security context and — if necessary —request for Annex 1 to be amended (see Article 55)*

support the involved companies in the upper end of the value chain, and will place them in an enhanced position versus their worldwide competition. Through their worldwide affiliations, the impact of the SENATE project will be felt outside Europe in America and Asia Pacific semiconductor centers and is expected to benefit the European economy tremendously by supporting its semiconductor equipment and IC sectors with innovations in manufacturing and export expenditures.

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