ARTEMIS Magazine is published by ARTEMIS-IA and ARTEMIS-JU. The magazine provides information on the developments within the ARTEMIS European Technology Platform, ARTEMIS Industry Association and ARTEMIS Joint Undertaking.

ARTEMIS

March 2010 NO.6 ~ ARTEMIS Spring Event 2010 & *embedded world 2010*

ENERGY EFFICIENCY

Making collaborative research work for you ~ Centres of Innovation Excellence ~ Embedded systems for energy efficient buildings Mobilising for automation in the European Process Industry ~ Possibilities for Cooperation between ARTEMIS and EIT?

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by Jan Lohstroh

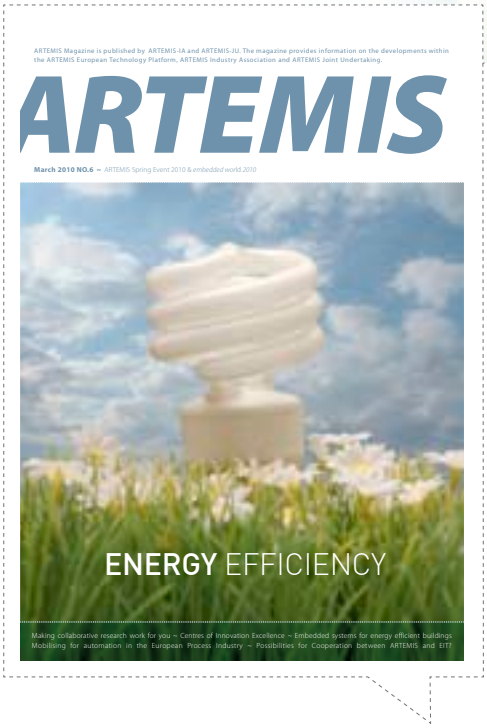
ARTEMIS-JU AUTONOMOUS ~ With the ARTEMIS-JU autonomous since October of last year, the ARTEMISIA Steering Board has decided that the ARTEMIS Magazine should be published jointly by ARTEMISIA and the ARTEMIS-JU. So this issue of the ARTEMIS Magazine is co-edited with Eric Schutz, Executive Director of the ARTEMIS Joint Undertaking, with both of us having an editorial column. For the next issues we might continue in this way or alternate.

ARTEMISIA → ARTEMIS-IA ~ Here and there in the articles you will notice that we like to stress the industrial orientation inherent in the ARTEMISIA acronym. When the ARTEMISIA association was founded, the ARTEMISIA acronym was originally intended to be ARTEMIS Industry Association, but in practice it became abbreviated to Artemisia. However Artemisia, as a name, is also a botanical genus of plants with 200 to 400 species (see: http://en.wikipedia.org/wiki/Artemisia). To separate us from the botanical meaning and to stress the industrial orientation of the association, we will gradually introduce a hyphen between ARTEMIS and IA to emphasise the Industry Association identity as originally intended. However, with the very essential (unchanged) subtext: "the association for R&D actors in the field of ARTEMIS". This implies ALL R&D actors as organised in the three ARTEMISIA chambers (SMEs, universities and institutes, and large enterprises).

ARTEMIS SPRING EVENT 2010 ~ ARTEMISIA has chosen to locate the Spring Event this year on the playing field of embedded world 2010 Conference&Exhibition. To underline the cooperation with embedded world we invited the embedded world chairman to write an introduction to his organisation and some of their key persons to write a technical article too. They chose to write on the subject of energy efficiency the leading theme of embedded world this year. The cover of this issue is a precursor to this important issue in the industry.

ECOSYSTEMS ~ A key topic for ARTEMIS-IA is to build self-sustaining innovation ecosystems for European leadership. So, special attention is recommended for the article of Yrjö Neuvo on page 8 and the articles about EIT ICT and ProcessIT.

FLOOR TO ERIC SCHUTZ ~ For the rest of this editorial page I give the floor to Eric Schutz to make his first editorial comments in this ARTEMIS Magazine issue now co-published byARTEMIS-IA and ARTEMIS-JU.



FOREWORD

by Eric Schutz

I was very happy when asked to contribute to this Editorial, the first of a new decade and the first full year of our autonomy. It's another way for me to express the importance of the balance that we have between the "Industrial" and "Institutional" partners in the ARTEMIS JU. Just like the successful collaboration between ARTEMISIA and the JU Office in the annual Brokerage Event for Call 2010, but more about that later.

The major milestone in 2009 was the autonomy of the JU Office. Prior to this, the experience of working side-by-side with their Commission colleagues stood our Programme team in good stead. This was particularly important when we autonomously ran the negotiations with the successful Call 2009 projects. The negotiations are a complex balancing act, where the best coverage of the programme, the benefit to participating countries and the optimum funding of partners all come into play. I'm happy that 13 projects were successfully negotiated. They are all introduced on pages 32-36.

With Call 2009 now concluded, we have Call 2010 in the starting blocks and the JU office team is ready to run once more. Sadly we are all facing the aftermath of the financial crisis, so the budgets that ARTEMIS Member States are able to commit are not as high as we would like. Still, we are confident that we can count on the positive spirit of all players, including the ARTEMIS Member States, to make the absolute best of available resources, even increasing these wherever possible, so that we can look forward to another truly excellent Call.

I'd like to thank all participants in ARTEMIS, whose huge efforts have got us to where we are today. Our team's goal is to serve the ARTEMIS cause and all its participants. Our doors, telephone lines and e-mail in-boxes are always open!

by Jan Lohstroh ~ *ARTEMISIA*

ARTEMISIA MAKING COLLABORATIVE RESEARCH WORK FOR YOU

ARTEMIS-IA, the Industry Association for all R&D actors in the field of ARTEMIS, is a membership association with two main goals: to manage the activity of the European Technology Platform for embedded intelligence and to represent the interests of industry, universities, research institutes and other interested parties in the ARTEMIS Joint Undertaking (JU).

GETTING STARTED ~ The story of ARTEMIS-IA started in 1994 with an initiative for a European Technology Platform (ETP) on Embedded Systems by European industry, the EC and 24 member states. Their reason for coming together was the need to develop and give momentum to a joint European vision and strategy on embedded systems. The stakeholders expressed the need to boost innovation and competitiveness among European companies and so create and keep jobs in Europe. This ETP became a Joint Technology Initiative: the ARTEMIS Joint Undertaking, a Public Private Partnership with ARTEMIS-IA the private partner.

INDUSTRY-DRIVEN PROGRAMME ~ To ensure that the ARTEMIS-JU programme is truly an industry-driven programme, the ARTEMIS-IA members propose research strategies with maximum short- to medium-term benefits for participating organisations. It ensures long-lasting benefits by encouraging projects with a high, positive impact on the target market. Collaboration among traditionally different domains is encouraged so that appropriate background technologies can be re-used across domains, shortening the innovation lead-time. It provides focus through "ARTEMIS Sub-Programmes", where group technologies and applications facilitate cross-domain collaboration. The content of the ARTEMIS sub-programmes is proposed annually to the ARTEMIS-JU by ARTEMIS-IA. Members can participate in the "Working Group SRA" to define topics and priorities. The ARTEMIS sub-programmes are also the seed of potential "innovation eco-systems": groups of complementary players who establish long-lasting collaborations to the mutual benefit of their respective businesses.

SHAPE THE FUTURE ~ ARTEMIS-IA's members may take an active role in Europe in creating a favourable environment for innovation in embedded intelligence. It offers its members a powerful forum to build strong partnerships with other participants in ARTEMIS-JU projects backed up by an on-line Partner Search Tool and first-hand information, giving members a considerable advantage when submitting proposals for competitive selection. The annual ARTEMIS Spring Event and Autumn Event guarantee the deployment of strategies and elections for the Steering Board and Presidium. In addition, they serve as live ARTEMIS meeting places where key industry players and other R&D actors identify topics for major R&D projects that they want to pursue together in response to the ARTEMIS-JU Calls for innovative proposals.

WHAT'S IN IT FOR YOU? ~ In just three years, ARTEMIS-IA has established an extensive network of potential partners with whom you can build your quality consortium. So teaming up with ARTEMIS-IA means that you team up with more than 185 companies and R&D organisations in Embedded Intelligence & Systems. Together you shape the R&D environment for ARTEMIS in Europe and make collaborative research work for you. But there is more.

ARTEMIS-IA members' additional benefits:

- Participation in Working Groups that define the strategies and content of all ARTEMIS activities
- Eligibility for election to the ARTEMIS-IA Steering Board and Presidium
- Free participation to regular ARTEMIS-IA events (Brokerage, Summer Camp, and more)
- Regular e-mail newsletters for members only
- Access to protected areas of the ARTEMIS-IA website and online Partner Search Tool
- Free copy of the ARTEMIS Magazine
- Make use of web tools that support dissemination of project results and logistics support for workshops and other meetings.

Save time and energy. Let ARTEMIS-IA membership give your company an innovation boost. ■

by Ad ten Berg ~ *ARTEMIS-IA Programme Coordinator*

ARTEMIS CENTRES OF INNOVATION EXCELLENCE

The ARTEMIS ambition is to establish and nurture "Centres of Innovation Excellence" (CoIE) as the central theme in its strategy as described in the Multi-Annual Strategic Plan. This strategic topic is the main focus of the ARTEMISIA Working Group CoIE introduced earlier in the ARTEMIS Magazine (no.4, July 2009, pages 24-25).

Since the Working Group was established in January 2009, it has been working towards a proposal to implement the CoIE strategy, a plan of concrete activities and processes. To remind you, the main purpose of a CoIE is to bring partners together in an open innovation setting combining inventions and marketing to stimulate economic growth and improve the competitiveness of its partners.

QUALITY MARK ~ Several ideas are being elaborated by the WG CoIE in a series of workshops and teleconferences into more concrete proposals. One of the ideas is to establish an ARTEMIS register for CoIEs that have obtained an ARTEMIS CoIE label. This ARTEMIS CoIE label will act as a quality mark that is supported by a formal assessment procedure according the rules and criteria established by the ARTEMISIA Steering Board. After assessment and a formal positive decision by the Steering Board, a CoIE will be able to call itself an "ARTEMIS CoIE".

The CoIE Working Group is currently defining the labelling criteria together with a label assessment procedure An ongoing long-term re-assessment procedure will safeguard that CoIE's still act according the label criteria a number of years down the line and so ensure that ARTEMIS maintains the high quality of the register of its CoIEs.

The ARTEMIS CoIE label criteria are still in the draft phase and need to be endorsed by the ARTEMISIA Steering Board, but a few examples of criteria can give you some idea of what they will contain. For instance, an ARTEMIS CoIE must include partners that compete in the market and a CoIE has to comprise all players in the supply chain - knowledge providers, generic technology providers, systems developers, systems integrators, manufacturers - and end-users. In addition, the geographical scope of a CoIE is expected to be regional or multi-regional.

The innovation and R&D in the CoIE are based on the strategy of "Open Innovation", fostering a culture of openness, trust, fairness and willingness to cooperate. External visibility is effected by means of common technology roadmaps and R&D strategies. Of course, the dominant R&D domain of the CoIE must fit the ARTEMIS SRA.

TOWARDS A LABEL ~ ARTEMIS also expects CoIEs to undertake specific activities that show that it acts as an entity with a shared interest that is externally visible. Some activities that will be proposed as elements of the labelling criteria are:

- to define a policy and to maintain an annually updated action plan that describes the main activities that drive the innovation system forward, such as common meetings, workshops, pre-studies/pre-projects, R&D projects, different interest groups (technology, sector, etc), events involving representatives from all stakeholders like researchers, developers, producers, users, financers, marketing, etc;
- to publish an annual activity and progress report that describes, among other things, the progress made on ARTEMIS label criteria;
- to provide networking and matchmaking facilities to encourage frequent interaction and the initiation of cooperative R&D projects.

Furthermore, the ARTEMISIA Working Group CoIE is also scouting for existing clusters or groups of cooperating companies and research institutions that could become potential CoIEs. Over the past year, it became clear that the Scandinavia-based ProcessIT Europe group wants to become an ARTEMIS CoIE. The CoIE Working Group is very pleased with this initiative since it encourages and sharpens the thinking process on CoIEs and their position in ARTEMIS. In the remainder of this article, ProcessIT Europe will present itself and explain the purpose behind its ambition to apply for the ARTEMIS CoIE label. ■

MOBILISING FOR AUTOMATION IN THE EUROPEAN PROCESS INDUSTRY

Efforts to create a research and innovation centre of excellence for automation in the European process industry has taken a big step forward following the recent meeting in Stockholm of industry, research and clusters along with public authorities. The intention is to create ProcessIT Europe, a Centre of Innovation Excellence (CoIE) targeting manufacturing automation within the framework of the European Joint Undertaking ARTEMIS.

"We have taken an important step towards realising **ProcessIT Europe** and expect to have all the pieces in place this autumn," says Professor Jerker Delsing of Luleå University of Technology and host of the meeting in Stockholm.

WIN-WIN ACROSS THE BOARD ~ ProcessIT Europe targets manufacturing automation for process industries like mining & minerals, pulp & paper, metals, oil & gas, energy, chemicals, pharmaceuticals and wastewater. Many of these industries share similar automation problems so there is a basis for making cross-industry solutions feasible. By targeting manufacturing automation for different industry sectors, ProcessIT Europe will have the potential to integrate automation activities now present in different technology platforms throughout Europe.

Industries, suppliers and end users will all benefit from ProcessIT Europe through increased competitiveness, enhanced product development and new business opportunities. The CoIE will focus on automation innovations enabled by embedded and information systems technology. In a growing global market where competition is increasing, such an initiative is both welcome and necessary.

The value proposition of ProcessIT Europe has a few key elements. Firstly, it will be a meeting point for manufacturing automation suppliers, their end users, active scientists and public authorities. Here, end user needs will merge with research and supplier competencies from which ideas for new products will emerge. These ideas will subsequently be incubated as R&D projects, with ProcessIT Europe serving specifically as an R&D project incubator. In parallel, the development of a road map for manufacturing automation within the targeted industries will support and influence other technology road maps by ARTEMIS and others.

BREEDING GROUND ~ Luleå University of Technology, together with the regional initiative ProcessIT Innovations, initiated the formation of ProcessIT Europe and hosted the recent meeting in Stockholm. Some 30 people, including representatives from automation suppliers, end users and regional clusters from Sweden, Finland, Poland, Germany and Austria attended. Representatives from the UK, Czech Republic and France have also announced their interest in participating in ProcessIT Europe.

It is quite natural and logical that the initiative to create a European ARTEMIS CoIE for IT in the process industry comes from the Bothnia Bay region, including northern Sweden and Finland, with its variety of heavy process industries and corresponding world-leading research. "Our research skills related to the

by Anders Johansson

The meeting, hosted by Professor Jerker Delsing of Luleå University of Technology, brought together some 30 representatives from around northern Europe.

"We believe that ProcessIT Europe also will attract more world-class researchers who can enhance Europe's status as a world-leading research region,"

Jerker Delsing

process industry go back a long way and we now have the ProcessIT Innovations research centre linked to the Luleå University of Technology and Umeå University. With some of Sweden's and Finland's key process industries, such as LKAB, Boliden, SCA, Stora Enso and Outokumpu Stainless, located in the Bothnia region, this is a breeding ground for top research," says Jerker Delsing.

Thanks to collaboration between research and industry stakeholders, ProcessIT Europe will be able to drive innovation processes whose social value will boost industrial development and elevate the quality of research. ■

By Yrjö Neuvo - *Former President ARTEMISIA*

ARE THERE POSSIBILITIES FOR COOPERATION BETWEEN ARTEMIS AND EIT?

Attending the ARTEMIS meeting at the end of October in Madrid was a very pleasant experience for me. ARTEMIS is making very good progress towards its ambitious goals. As my major "hobby" is now the European Institute of Innovation and Technology, where I am a member of the governing board and its executive committee, it is interesting to take a look at possible areas of cooperation between ARTEMIS and EIT.

Yrjö Neuvo

THE KNOWLEDGE TRIANGLE ~ The foundation of the EIT is the knowledge triangle: education, research and innovation. EIT has a significant amount of autonomy in its operations (EIT is a Community Body, a bit like ARTEMIS). The most visible form of EIT's activities will be the Knowledge and Innovation Communities, or KICs. These are tightly integrated, focused and managed entities that implement the knowledge triangle in their specific fields. Each KIC is comprised of maximum six co-location centres each having a crystal clear role within the KIC. The KIC is not yet another cooperation network. Rather, by focusing on long-term and close cooperation across the co-location centres and among the participating universities, companies and research institutes, new competencies, innovations and companies are created. Entrepreneurship is very high on the EIT's agenda.

MOST LIKELY CANDIDATE ~ Around a quarter of the funding for KIC activities is expected in time to come from the Commission, with the rest from other sources like European, international and national programmes. This naturally opens up the possibility to cooperate with ARTEMIS. Last December the first three KICs were selected covering climate change, sustainable energy and future information and communication society. As embedded systems are already omnipresent today, and tomorrow even more so, in principle it is possible for any of the selected KICs to cooperate with ARTEMIS. However, the most likely candidate is the ICT KIC.

EXPLORING THE SYNERGIES ~ Personally, I would like to see cooperation being established as I see the JTI and the EIT approaches as nicely complementary approaches and, at a bit more detailed level, the synergy question lies somewhere between the plans of the co-location centres and the ARTEMIS sub-programmes. It is easy to see why some of the parties are already active in both ARTEMIS and the EIT ICT Labs, although any form of cooperation is completely in the hands of the two parties.

Establishing Centres of Innovation Excellence (CoIE) has been on the ARTEMIS agenda for some years. As far as I understand, the objectives of the CoIEs are rather similar to those of the KICs. An interesting question is: could a KIC or one of its co-location centres become a CoIE? My answer is, in principle, yes. This could even be highly beneficial! It is clear that a KIC has already solved some of the challenges that establishing a CoIE would face. Are there enough synergies for moving forward? As the EIT ICT Labs has now been selected as the ICT KIC, this definitely is worth checking. An answer to this could be achieved in a matter of hours. ■

by Magnus Madfors

EIT ICT – BRIDGING THE GAP TO OPPORTUNITY

EIT ICT Labs, a consortium of five European ICT innovation centres, was selected in December last year as the EIT-KIC in the area of future information and communication society. An EIT-KIC is a Knowledge and Innovation Community whose aim is to bring together universities, research institutes and industries in Europe to improve innovation and to bridge the knowledge gap between all actors. Committed to an efficient open innovation model, EIT ICT Labs will generate faster transformation of ideas and ICT technologies into real products, services and business, boosting Europe's future competitiveness in order to compete with other innovation hotspots in the world.

NEW BUSINESS PROSPECTS ~ EIT ICT Labs builds upon five geographical co-location centres – Berlin, Eindhoven, Helsinki, Paris and Stockholm – each of which combines world leading companies with globally renowned research institutes and top-ranked universities along with strong national and regional support. In addition, EIT ICT Labs also has associate partners in Budapest, London and Trento. We will establish a new partnership between business and academia based on trust, transparency and mobility of ideas and people by connecting partners, together covering the entire value chain in the ICT sector. This will help capture new business opportunities in the dynamic ICT sector and so become an important initiative in accelerating new ideas to market as well as fostering new competences in the areas needed.

INSPIRING ENTERPRISE ~ Our mission is to grow and capitalise on the innovation capacity and capability of actors from higher education, research and business from the EU and beyond, thereby addressing Europe's innovation gap through the concerted efforts of all facets of the knowledge triangle. Our aim is to inspire creative students, researchers and business people to embrace risk-taking and adopt an entrepreneurial attitude, which will promote the identification of new business opportunities and turn Europe into a knowledge society.

EIT ICT Labs will be fully operational in 2010 through the formal establishment of our organisation, including governance and implementation at our five co-location centres. The presentation of a first triennial work plan together with a strategic innovation agenda will be the starting pistol for launching programmes and projects during the second half of 2010 that will see partners cooperating. ■


ARTEMIS
Spring Event
Joint located with embedded
world 2010 Exhibition&Conference

Energy Efficiency

EMBEDDED SYSTEMS PEOPLE NETWORK IN EUROPE; THIS TIME WE NETWORK WITH EMBEDDED WORLD 2010

Klaus Grimm
President of ARTEMIS Industry Association

Klaus Grimm started his career with AEG, the electrical/electronic company, working on reliability calculations for technical equipment. In the mid 1980s, he shifted into software engineering. In 1989, AEG Research became part of Daimler-Benz. Daimler concentrated the whole of its research in one division, thereby giving Dr Grimm the opportunity to work not only for AEG but also on space/aerospace, automotive and defence electronics. "This was a really fascinating period where I got to know the different application areas of embedded systems – not only AEG equipment but also planes, satellites and cars." Klaus Grimm later became head of the Daimler Electric/ Electronics & Software Technology Laboratory in Germany.

The ARTEMIS European Technology Platform, continued by the ARTEMIS Industry Association (ARTEMIS-IA) since 2007, has always been actively involving as many key players as possible in Europe to develop the best strategy for Europe to excel in embedded systems. Since 2008 an annual co-summit has been organised with ITEA2, as part of the annual ARTEMIS Autumn Event. ARTEMIS-IA also organises a yearly Spring Event for its members, in co-location with an important ICT event in Europe where possible.

Following last year's co-location with the DATE2009 Conference in Nice, this year we are cooperating with the *embedded world 2010 Conference & Exhibition* in Nürnberg. An important element of this cooperation is that a select set of ARTEMIS projects is being presented in a special session of the *embedded world* conference, open to all participants of this conference and participants of the ARTEMIS Spring Event.

The organisers of the *embedded world* congress consider the ARTEMIS special session a highlight. The audience of the ARTEMIS Spring Event 2010, which takes place in the eastern wing of 'the Messe', will move to the conference floor in the west wing for the ARTEMIS session. The industry-driven ARTEMIS Programme aims to boost the efficiency of technological development and, at the same time, enhance European market competitiveness in the supply of embedded systems technologies. ARTEMIS nurtures the twin aim of a strong European position and world-class leadership in embedded intelligence and systems. It is hardly surprising, therefore, that we are indebted for having the opportunity to provide insight into the world of ARTEMIS: Advanced Research & Technology for EMbedded Intelligence & Systems.

We appreciate this cooperation with *embedded world*, which complements the ARTEMIS network with the vast network around the *embedded world* exhibition and conference. We especially value the creative enthusiasm of Professor Sturm and the crew of the *embedded world* organisation in also supporting our Spring Event, in my opinion a good basis for other options for future collaboration. In this context we value the contribution of Professor Sturm to our magazine in which he presents the activities of *embedded world* along with his vision on the cooperation with ARTEMIS-IA. We are also grateful to the members of the Vendor Expert Board of *embedded world* that have contributed articles on subjects related to energy efficiency, the lead theme of *embedded world* this year. The cover of this issue of the ARTEMIS Magazine is illustrative of the content of these articles.

by Professor Dr.-Ing. Matthias Sturm ~ *Chairman of the embedded world 2010 Exhibition&Conference and member of the Vendor Expert Board*

... IT'S PEOPLE WHO GET PROCESSES SOMEWHERE

Prof. Matthias Sturm

Professor Matthias Sturm studied at the Technical University of Mittweida electronics technology. From 1981 he worked in various companies in the field of robotics and switched in 1985 to the Technical University of Leipzig. Here he developed microcontroller based instruments for science. In parallel, he worked on his dissertation in the field of nuclear instrumentation, which he conclude successfully 1992 with the title Dr.-Ing.. In 1993 he was appointed Professor of Microcomputer and Electronics at the University of Applied Sciences Leipzig (HTWK) and exerts this activity so far. Since 1996 Prof. Sturm organised congresses on embedded systems development. He demonstrated his ability as an expert in the field of embedded system development by lectures and publications so he has won the recognition of the embedded community. Since 2003 he leads the advisory board of the 'embedded world – exhibition and conference' and is responsible for the content of the embedded world conference. In 2006 Prof. Sturm was voted as one of the ten best Professors of Germany in the field of engineering science.

HOW DID *EMBEDDED WORLD* GET OFF THE GROUND? ~ *embedded world* made a flying start when it was first staged in 2003. Looking back I'd say there were a number of reasons for its success. *embedded world* was meant to be an exhibition plus a conference, so it's an excellent meeting place for the entire sector, with its interesting combination of product presentation and knowledge transfer. In NürnbergMesse you have two organisers whose commitment to the exhibition and WEKA FACHMEDIEN for the conference has impressed the embedded systems community. The nomenclature of the *embedded world* Exhibition & Conference has barely changed since its inception. The focus on a tightly wrapped selection of subjects, comprising hardware, software, tools and service, is doubtlessly another point that has contributed to the success of the event. But what I feel to have been quite essential is the acceptance of *embedded world* by visitors to the exhibition and conference. Highly qualified engineers from different fields of embedded systems development have made this their embedded event. Even a substantial increase in exhibition space and the numbers of visitors and participants couldn't rob the *embedded world* of its almost family character. Quite the contrary, more and more it's becoming a working event where the brightest brains in the sector meet to generate innovative and creative ideas.

The *embedded world* Exhibition & Conference has witnessed economic ups and downs in the meantime but has remained largely unaffected by them to become a leading world stage for embedded systems.

HOW DID *EMBEDDED WORLD* BECOME WHAT IT IS? ~ The development of the *embedded world* Exhibition & Conference can be judged from the facts and figures for the 2003 and 2009 events. But briefly: in 2003 we welcomed 353 exhibitors and in 2009, 704 exhibitors. The conference started in 2003 with 583 participants from 19 countries and in 2009 we saw a growth of 1.023 participants from 53 countries. Nowadays one can say that we are one of the biggest events in the world.

WHAT'S THE FOCUS OF *EMBEDDED WORLD* THIS YEAR? ~ Innovation in the sector continues unabated, growing year by year, though the focal points are always shifting a little. Automotive applications are taking more of a back seat at the moment while medical technology is undergoing strong growth. The energy efficiency of embedded systems looks like being a major theme at this year's event. There are numerous approaches to confronting the current problems facing the world, with intelligent and rational solutions. The Vendor Expert Board of *embedded world* has consequently devoted its report this year to the subject of the "Energy efficiency of embedded systems" (see page 11-19).

WHICH WAY IS *EMBEDDED WORLD* GOING IN THE NEXT FEW YEARS? ~ Everyone involved – and here I mean not only the exhibition and conference organisers but, in my role as board chairman, also the exhibitors and visitors – wants to expand and strengthen the standing of *embedded world* as a leading world stage. Europe is a very good place to be undertaking this, and especially Nuremberg, situated as it is at the centre of Europe. Our sector is very dynamic and used to moving within a changed framework with different accompanying factors. And that's exactly the way it is with *embedded world*, true to the motto: "You have to change to remain true to yourself".

HOW DO YOU SEE COOPERATION WITH ARTEMISIA, NOW AND IN THE NEAR FUTURE? ~ I think a great deal will come of cooperation with ARTEMISIA. Actually I wonder why we didn't team up earlier. ARTEMISIA's objectives of bringing leading industrial and R&D actors together, of identifying and promoting cross-national research topics, are exactly in line with the interests of *embedded world*. Especially as we're able to welcome the same partners at our event, leading enterprises and researchers. I'm sure that the two, ARTEMISIA and *embedded world*, will turn out to be an excellent match, and I would even suggest that ARTEMISIA's Spring Event always be held parallel to *embedded world*. There's hardly any other opportunity of gaining such a compact impression of the capabilities of our community. And the possibility of learning from the experience of researchers and developers gained in the course of ARTEMISIA projects would definitely be much appreciated by those attending the exhibition and conference. I'm also very pleased to see that the world of politics has, in the meantime, discovered the enormous potential of embedded systems. Here, too, close cooperation with ARTEMISIA can be very rewarding.

We need to remember that it's people who get processes somewhere, people who have to meet, despite all the advanced technology we have at our disposal. And what place could be better than a joint *embedded world* event in Nuremberg? ■

by S. Lauterbach ~ member Vendor Expert Group *embedded world 2010*

NEW CHALLENGES FOR DEVELOPMENT TOOLS

The complex debug infrastructure of multicore SoCs (see figure 1) and their advanced low power modes present the current challenges for debugging tools.

Multicore debugging has different requirements for AMP and SMP systems. In asymmetric multiprocessing (AMP) the tasks are assigned to specific cores during the design phase that may use different architectures and separate memory subsystems (heterogeneous multicore). From a debug tools view AMP means debugging each core in a separate view.

Stephan Lauterbach

Stephan Lauterbach is General Manager at 'Lauterbach", responsible for Debug & Trace tools development. As a co-founder of Lauterbach he has a deep knowledge of debug technology ranging from classic In-Circuit Emulation systems of the past to complex Multicore SoC debug and trace architectures of today. He is a member of MIPI Test&Debug and also involved in other industry organisations.

In symmetric multiprocessing (SMP) the tasks are assigned to an array of cores of the same architecture in which the same memory (homogenous multicore) is shared dynamically by an operating system. Multithreaded cores can be seen as a special SMP system case. For debugging it does not matter if the different cores execute code in parallel "really" or just "virtually". From a debug tools view SMP debug means looking at all cores from "one" view and trying to "hide" the multiple cores whenever possible.

The boundaries between AMP and SMP systems are in reality not so sharp. SMP systems may have some level of "asymmetry" while AMP is often implemented on top of SMP hardware (as shown in figure 1).

AMP SYSTEMS ~ Asymmetric multiprocessing has been used in embedded systems for quite a long time now. SoCs often consist of a standard controller (usually a RISC architecture) running the main software stack and specialised accelerators (DSPs or customised cores), a normal configuration for mobile baseband chips or cable modems. These cores typically come from different IP vendors that tend not to share the same debug and trace concepts. The need for correlated debug and trace and the limited number of available pins means that multiple debuggers in parallel only cannot be used. An integrated concept that can access all debug resources through one interface is required. This integration is done by custom components (like chip level TAPs or cross-trigger logic as shown in figure 1) or configurable IPs (like ARMs CoreSight, NEXUS-5001, MIPI-STM or JTAG 1149.7). What features are supported and how this is done are up to the chip designer. Flexibility and modularity of the debug tool is required to support the variety of combinations of these technologies.

SMP SYSTEMS ~ Symmetric multiprocessing is a relatively new approach for embedded systems. In this case one operating system can split the work across a number of cores during runtime. In theory SMP debug support seems to be simpler – there is just one architecture and one operation system (assuming no virtualisation). But in reality there are a lot of pitfalls in existing implementations, some of which are the result of the SMP as such and some simply implementation issues concerning existing chips. In terms of the former, the problem is how to visualise the simultaneous hit of breakpoints on multiple cores to the user? Where the cores have no truly synchronous stop capability, this problem can even be compounded by implementation and produce situations where only one core executes code during debug. Can the software on the target tolerate this? Tracing the execution flow of an SMP system and analysing the system performance is another challenge. Tracing multiple cores is not a major problem – it is just a question of available trace port bandwidth. Getting

simple interpretable results and providing different views from "high level" (application flow) to "low level" (instruction level) is the focus of work today.

POWER SAVING MODES ~ In the past saving energy on SoCs was done by switching off or reducing the clock rate for parts of the chip. The size of the new SoCs and the small process geometry result in high leakage currents. This requires new power management concepts that include powering down those non-operating components of the chip. This, of course, also affects the debug infrastructure. Traditionally JTAG debug for multiple cores was done by just connecting all the cores of target access ports (TAPs) in a chain but powering down one core would break the chain. Different concepts have evolved to tackle this problem. Chip level TAPs (sometimes also called "scan chain manager") can bypass powered down components in the JTAG chain. Bus-based debug concepts – like ARM´s CoreSight – avoid the problems of the broken JTAG chain completely. The bus just needs to isolate the powered down cores.

Debug and trace through such a power cycle is another challenge. Two solutions are available here. If just one core is powered down, then the target can save and restore the debug resources (e.g. hardware breakpoint registers) in a memory that keeps the contents. After re-powering the core, it first restores the debug registers before handing over execution to the application. If the whole target is powered down and restarted (quite common in automotive or hard-disc applications) then the debugger has to monitor the power lines and restore all registers in the target when power resumes. Ideally this is done while the power on reset is active so that the behaviour of the target does not change at all. ■

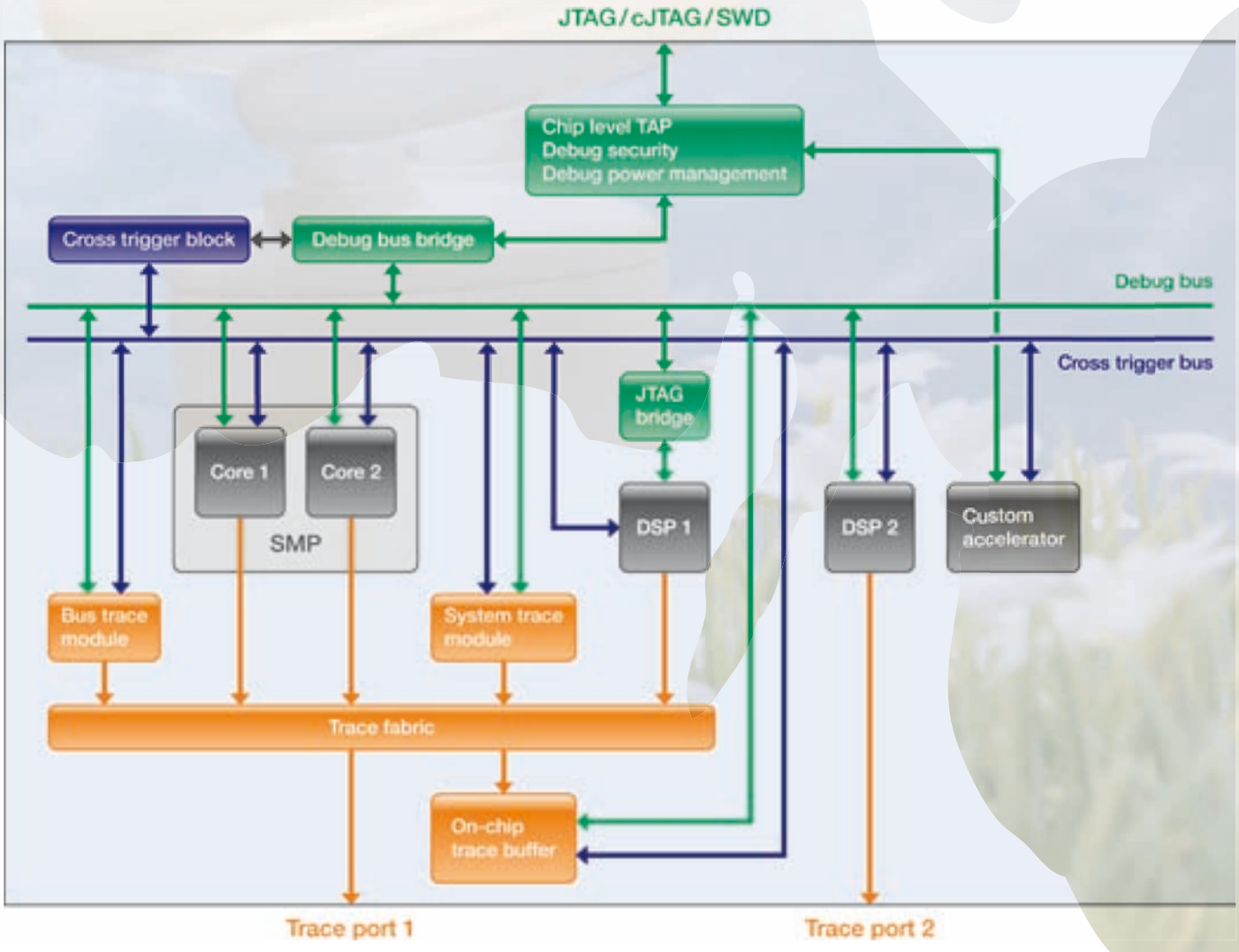


Figure 1: Example debug infrastructure of a multicore SoC

by Reinhard Keil ~ *member Vendor Expert Board embedded world 2010*

SOFTWARE DESIGN FOR MICROCONTROLLERS

The next generation microcontrollers will offer even more feature-rich peripherals, energy saving capabilities and operating modes that address safety requirements. Memory sizes and the performance of single-chip microcontroller systems allow the implementation of real-time operating systems, software stacks for sophisticated communication protocols and graphical displays. Even the instruction sets of microcontroller cores are being extended with digital signal processing capabilities. This modern microcontroller hardware is cost-effective and combined with the new features will enable many new application areas such as home automation, energy optimisation or device networking. However, for application programmers it will present new challenges that are not just measured in increased program size.

Today, microcontroller applications are monolithic programs composed by small software teams. Most software components are developed in-house and code-reuse is limited to modules that are created within the same company. Application software is frequently based on reference designs provided by silicon vendors, but complex software components are seldom purchased from independent third-party companies. Typically, an integrated development environment (IDE) with an ANSI C compiler and a target debugger is used as the software development platform.

FRAUGHT BY FRAGMENTATION ~ The MCU market is one of the most fragmented in the today's electronics industry, with at least 100 different microcontroller architectures available. These architectures have been cost-optimised over time but have restrictions, each requiring a different set of development tools and therefore specific training for the embedded software engineer. The situation is similar to the computer industry before the introduction of the PC: programmers had to invent individual solutions time and again for very similar computing challenges and adopt existing software algorithms to new hardware since no peripheral or interface standards existed. Nowadays, generic software components are commonplace in the PC world.

Several microcontrollers are still based on 8- and 16-bit architectures with specialised instruction sets and memory limitations. Consumer demand for more product features, together with technology enhancements and silicon price erosion mean that 8- and 16-bit devices are no longer attractive for new product designs. The trend is towards 32-bit microcontrollers that are designed for real-time operating systems and object-oriented programming techniques. This by itself allows better software structures. And to address the needs of safety-critical applications, several 32-bit architectures incorporate a memory protection unit (MPU) which detects software access failures.

TREND TOWARDS STANDARDISATION ~ Many of the next-generation microcontrollers are based on the ARM Cortex-M processor series. Third-party IP such as this helps MCU vendors bring down development costs and, therefore, there is a natural trend in the silicon industry to standardise on widely used processor cores. The same set of development tools can be used for all microcontrollers based on such standardised cores, even when devices have different peripherals or are supplied by various silicon vendors.

Additionally, to achieve a consistent software platform and cut software costs, ARM and members of the ARM ecosystem have introduced the Cortex Microcontroller Software Interface Standard (CMSIS), which enables silicon vendors and middleware providers to create software components that can be easily reused.

Standardised processor hardware, along with common software programming guidelines, creates the foundation for the next level of

"Development tools can support modular plug-in applications even for smaller embedded systems"

Reinhard Keil

Reinhard Keil is the Director of MCU Tools at ARM. His responsibilities include the definition and strategy of tools for ARM Microcontrollers. He is founder of Keil Elektronik GmbH (the German root of Keil Software Inc.) and co-author of several key software products, such as Keil C51, Keil C166 and µVision. Reinhard continues to influence the microcontroller market and to advance the technology of the embedded space.

software abstraction in the deeply embedded industry. Filter design utilities combined with optimised libraries can replace analog components while providing even better long-term stability. Today's RTOS kernels will be expanded to directly support the various microcontroller power-saving features. RTOS layers for plug-in applications use the MPU to protect the safety-critical parts of a system. Components such as graphic library, file system, TCP/IP, USB OTG, or wireless communication stacks can be purchased from third-party companies. This will even allow web services or tiny database systems to run within a microcontroller application.

NEW DESIGN APPROACH ~ Development tools can support modular plug-in applications even for small embedded systems. This will replace today's monolithic approach. As this happens, the application programmer will become a system architect creating the software with new design methods such as the Unified Modelling Language (UML) that ensures a clean data communication structure, controls RTOS features and even specifies the critical execution times of an application.

This new design process will have the potential to simplify system validation. With the debug and trace features of modern 32-bit microcontrollers, code coverage is fully supported and ensures a more complete software test. Third-party plug-in applications can be pre-verified and their wide usage ensures better overall quality. Combined with new design methods and tools for software test automation, a complete application can be more easily validated and certified.

Several of the outlined concepts are still visions. However, the on-going standardisation of microcontroller hardware and software components is likely to make them reality in the near future. ■

by Horst Diewald ~ *member Vendor Expert Board embedded world 2010*

EMBEDDED CONTROL – ASPECTS OF ENERGY EFFICIENCY

Energy efficiency has been a key criterion for applications like calculators, real-time clock systems, heat meters, etc. for more than 40 years. Portable equipment for entertainment and communication aroused broad public interest and the development of markets and technology for "music everywhere" and "be connected anytime, anywhere" has been driving demand for much more efficient use of the energy.

System design and energy management along with embedded software and debug requirements are having to provide adequate responses to the increased complexity of semiconductors and features of size. Three aspects are considered here: the architecture of the embedded controllers, the software that runs on such controllers and the debugging challenges.

USE OF ENERGY ~ The term 'use of energy' is defined as the energy that is taken from the energy source, e.g., a battery, according to the formula E = V * I * t = P * t.

In many embedded systems the controller needs to operate only for a portion of the time. The various power-down modes are used in conjunction with proper start and stop capabilities to optimise the use of the available energy. The multiple low-power modes provide shut-down capability of those parts of the microcontroller that are unused by the actual function.

ACTIVE MODE AND POWER-DOWN/ SLEEP MODE CONSUMPTION ~ The energy consumption in early ultra-low power implementations was focused on the current consumption and time of operation, keeping both as small as possible. The focus on active mode current consumption has been on the DC current, mainly used from analog circuits, and the AC current, coming from switching activities. The sleep mode current consumption is driven by "leakage" current and the remaining operational current consumption like calendar or liquid crystal display function. As the process scaling proceeds, the energy consumption (or loss) becomes critical in ultra-large scaled integrations and ultra-low power systems. Both end in similar processes, circuit designs and system solutions.

IMPLEMENTATION CONCEPTS FOR EFFICIENT USE OF ENERGY ~ The DC current can be reduced, or at least well controlled, by switching a portion of the embedded controller into low-power modes, disabling them or even switching them off. The permanent available functions have to be optimised for low energy consumption as in the watch crystal oscillator along with the calendar function that remains operational even during the lowest power-down mode.

The AC current is mainly dominated by the parasitic and its frequency of charging during the operation. The parasitic is reduced through keeping the circuits small for a given function and close together in layout. The clock gating enables toggling activities only for the time the operation is needed; for all other times energy saving occurs. The clock is gated, if feasible, at the source. This prevents energy consumption by the

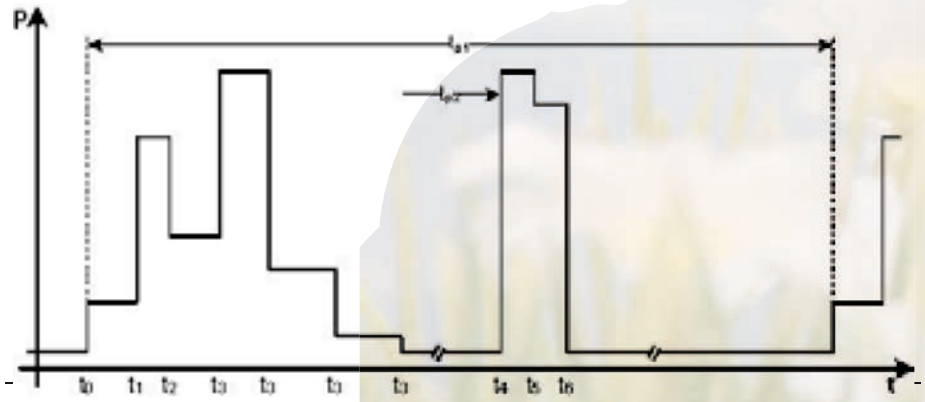


Figure 1 The knowledge of the power profile of the target application enables the most efficient use of energy.

Horst Diewald
MSP430 Chief Architect
Distinguished Member Technical Staff

Horst Diewald is the world-wide Chief Architect of the MSP430 core, with responsibilities in system and product definition. In his WW role, Horst's main focus is on the future evolution of the MSP430 architecture, the "ultra-low-power" and analog features.

During his career at TI, Horst developed the architecture of the MSP430 with a team of engineers. He defined the CPU core, wake-up and interrupt scheme, bus architecture and peripheral system to optimize ease-of-use, high performance at lowest current consumption, and system cost of the MSP430. He holds the basic patent of the low-power scheme, and is co-inventor of the basic patent of the low-power and fast clock scheme which enables "burst-mode" concepts. He also holds a patent for the integrated FLL oscillator concept, among others.

He was elected Member Group Technical Staff in 1991, Senior Member of the Technical Staff in 2000, and Distinguished Member of the Technical Staff in 2003

Horst is affectionately known within TI as 'The Godfather of MSP430".

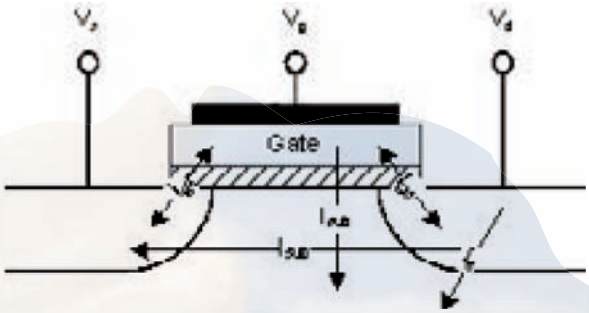


Figure 2. The value of the different leakage currents vary between the CMOS process technology, substrate, sub-threshold and gate leakage.

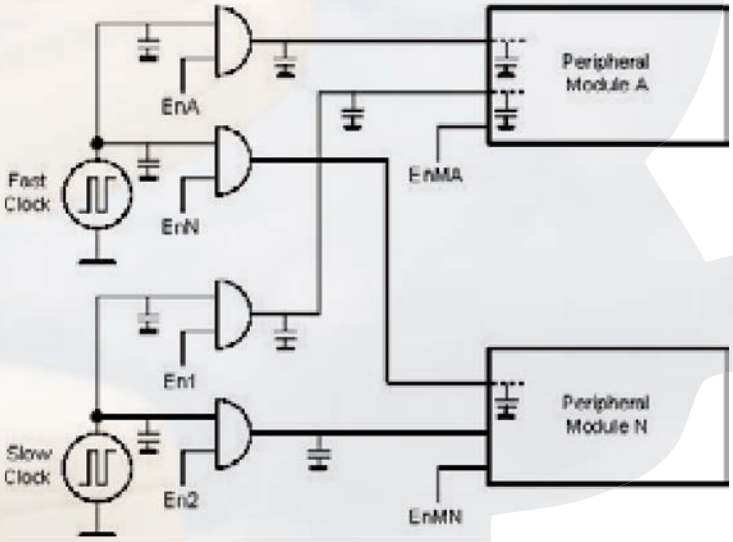


Figure 3. The active mode current is controlled through controlled oscillators and intensive clock gating. Toggling of nodes is minimised to the actual need for proper operation.

wiring parasitic capacity. This is an example of the overall system and chip design along with low-power library support having an important influence on the effective parasitic, resulting in AC current consumption.

The leakage currents dominate the sleep/low-power current and, in most advanced processes, they also contribute to the current consumption during active mode. Depending on the final energy budget, the power management can become much more sophisticated. The general trend is towards complex power and clock gating, extended support from the process technology and smart system partitioning in the integrated circuits and embedded controllers. Key concepts include high or multiple VT transistors and power-optimised libraries, high-k gate processes, dynamic voltage-frequency scaling and integrated oscillators.

Overall, the general move to low-power embedded processing controllers will continue with new hardware functions, communication, audio and video capabilities, and increasing software size and processing demands. ■

by Jose J de las Heras & Rafael Socorro

EMBEDDED SYSTEMS FOR ENERGY EFFICIENT BUILDINGS

As the title suggests, the eDIANA project focuses on the building sector and scalable concepts to assess, handle and optimise energy consumption in Cells (living/working units) and MacroCells (residential and non-residential buildings). This three-year project, financed by the ARTEMIS Joint Undertaking and respective national public authorities under the ARTEMIS Call 1, kicked off February 2009.

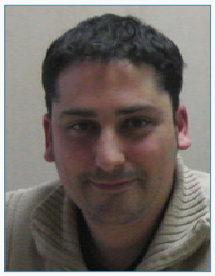
Rafael Socorro
ACCIONA INFRAESTRUCTURAS RESEARCH AND DEVELOPMENT Information and Communication Technologies - Spain

Mr. Rafael Socorro was born in the Canary Islands, Spain. He graduated from Polytechnic University of Valencia in Telecommunication Engineering. He joined ACCIONA Infrastructures in 2007 as a Project Manager and since then, he has been involved in several National and European R&D Projects regarding the use of ICT for energy efficiency in buildings. Currently, he is mainly focused in embedded systems technologies in construction and the promotion of standardization for embedded systems.

MULTI-FACETED, MULTI-PURPOSE FRAMEWORK ~ The aim of eDIANA is to prepare a novel framework to support system analysis and engineering with component models and tools that enable the interoperable exchange of information leveraged by new energy management algorithms. The development of a real-time power consumption sensor and embedded energy controller for urban and domestic environments will not only reduce energy demand but also allow utility companies to more effectively manage energy load and allow consumer to adjust consumption and to make real data-based decisions. The picture that emerges will be an urban or residential world where electricity can be accessed, read, profiled, curtailed and managed for various devices, with an increasingly precise response to changes in weather, user comfort, security criteria, demand and price.

Moreover, eDIANA middleware infrastructure will introduce novel algorithms, protocols and software tools that enable interaction among heterogeneous devices, satisfying the required energy management functions and operations through collaborative and context-aware devices at different levels of the architecture. The delivery of these innovations in the home, office and building domains, based in a coherent system platform as the proposed by eDIANA and aligned with the proposed reference architecture and derived examples, will be key to delivering effective energy management functions across the European urban landscape. As a result, the whole value chain (users, producers, operators, building-related companies and embedded technology providers) benefits from the envisioned interoperable middleware infrastructure.

MODEL-BASED DESIGN ~ As already mentioned, the application of model-driven engineering for embedded systems, in the context of eDIANA, provides a systematic approach to the specification, design, development and delivery of complex systems that attempt to separate system architecture views from design and realisation technologies. This allows architecture and device-level software and hardware-specific design to evolve more or less independently. Model-based design can raise the level of abstraction from the realisation domain to the problem specification domain, which means we can reason about the general



Jose J de las Heras
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Mr José-Javier de las Heras is currently working at ACCIONA R&D Department as a project manager and Head of the ICT Division. His main fields of interest are embedded systems, wireless sensor networks and ambient intelligence for more efficient and smarter construction processes. Besides his role as coordinator of eDIANA project, he is currently involved in the FP7-REEB project, in charge of establishing the European vision and roadmap for future R&D in ICT supporting Energy Efficiency in the Built environment. In the past, he has been involved in many CELTIC (CBDP, ENCOMPAS2) and ITEA projects (ESNA). He has been the coordinator of a National Project called FUTURESPACIO, in charge of integrating ICT-based solutions in the construction sector. He has been the Smart Buildings Advisory Group Chairman for the European Commission. He is one of the authors of the ECTP "Processes & ICT" Focus Area Strategic Research Agenda and the ARTEMIS Research Agenda.

properties of the design rather than a specific implementation under a given (fixed) software/hardware partitioning. This is key to eDIANA as it provides the means to address challenges such as robustness, diagnosis and maintenance from a trade-off analysis perspective. So, given appropriate methodologies and tools, such models can be synthesised into efficient, reliable software and hardware realisations with the potential to radically improve design productivity and the quality of the whole set of embedded elements to be developed under the eDIANA project.

ROBUSTNESS ~ In order to produce and assess robust elements for the eDIANA Platform, product development, support and after-market engineers require a framework to distil physical parameters from the environment and compare them to a model-based view. While the effect of a single failure in the proposed eDIANA Platform is not critical, the large-scale deployment of energy-efficiency management embedded systems in urban areas could mean that single failures, repeated across a large number of installations, have a significant impact on the whole energy management system. Therefore, the eDIANA model-based simulation framework must assess the capability of an energy-efficiency management component to deliver an acceptable level of service within the overall architecture despite the occurrence of transient and permanent software and/or hardware faults, design faults, imprecise specifications and accidental operational faults.

A few previous projects have addressed the design of solutions that integrate legacy systems and smart environments, sensors nodes, electrical appliances and home appliance to improve energy efficiency and optimise overall energy consumption, production and storage in a building, exploiting real-time measurement and control. However, no projects have dealt with the study of architectures, topologies and communication protocols in scenarios where heterogeneous networks are present. eDIANA addresses the design of all relevant embedded technologies, and the implementation and testing of all the complete systems needed from sensor devices to information gathering and exchange.

Last but not least, eDIANA is geared to three standardisation areas that focus on future relevance: building-relevant standards regarding energy and home automation, communication (e.g. between system components and Cells) and safety. Furthermore, eDIANA is examining emerging interdependencies and coherences between these different areas that are currently being considered separately. By systematically identifying and presenting the relevant state-of-the-art standardisation and impact on future work in standardisation and research, eDIANA aims to develop a future-oriented product that will have the support of all stakeholders. ■

by Dennis Alders ~ *Coordinator SCALOPES*

EMBEDDED SYSTEMS ARE "ENERGY CHALLENGED"

The goal of SCALOPES is to enable an industrially sustainable path for the evolution of low-power multi-core computing platforms for application domains with strategic value for European competitiveness. The technical innovations are driven by and proven for four different application domains: communication infrastructure, surveillance systems, smart mobile terminals and stationary video systems. The project is financed by the ARTEMIS Joint Undertaking and respective national public authorities under the ARTEMIS Call 1. It started in January 2009 and runs till December 2010

HIGH PERFORMANCE, LOW POWER ~ The design of modern embedded systems is often beset by conflicting requirements, like the simultaneous need to be low power while providing high performance, so power optimisation is one of the driving themes in the SCALOPES project. Examples include battery operated (wearable) portable devices suited for the display of streaming video and non-portable, power-rich platforms as in television sets, where the packaging and reliability costs associated with high power and high performance systems also force designers to look for ways to reduce power consumption. In fact, embedded systems are "energy-challenged" at all levels.
The application behaviour of modern, typically software-centric, MPSoC-based embedded systems is becoming more and more dynamic, with two distinctive types of dynamic behaviour: intra-application and inter-application. Intra-application dynamic behaviour relates to the different behaviours, or operation modes, of a single application. For example, a video application could dynamically lower its resolution (and thus its QoS) to decrease its computational demands in order to save battery life. Inter-application dynamic behaviour, on the other hand, refers to the fact that modern embedded systems often require to support an increasing number of applications and standards. In order to cope with the dynamic behaviour, system-level design is used to raise the abstraction level of design. This approach allows the capture of multiple applications during system design.

The increased complexity of MPSoC design has led to a way of designing SoCs that takes account of composability, predictability and dependability. Composability enables the development of stable software for very large SoCs by ensuring that parts of the SoC software can be developed and verified separately. Predictability ensures that the tools that calculate the timing behaviour enable the correct design and scaling of systems to ensure that the real-time conditions are met. Last but not least, dependability relates to the behaviour of the system in the event of errors or problems during operation.

SEAMLESS ADAPTABILITY ~ The challenge in designing a Resource Manager (RM) for multi-core platforms is to adapt seamlessly, during run-time, to the power consumption and the overall performance of the architecture according to the application needs and its surrounding environment.
A common RM is structured around two entities: the Local Resource Manager (LRM) and the Global Resource Manager (GRM). The LRM encapsulates the local policies and mechanisms used to initiate, monitor and control computation on the corresponding domain while the GRM manages jobs (a group of communicating tasks allocated on a domain). In other words, the RM supports both platform scalability and application scalability.

Ongoing RM design is characterised by two approaches. The first shares a common application between two platforms – a symmetric multiprocessor running SMP Linux versus an asymmetric multiprocessor platform. The second approach makes use of a single platform running Linux providing support for System Control State Machine (SCSM) and Dynamic Frequency Scaling (DFS). Power aware design technologies and methods will create a unified framework supporting the design of complex, heterogeneous, reconfigurable, multi-core systems optimising the use of the available resources in terms of power consumption, performance and reliability. A multipurpose

board is being developed for high-speed network monitoring, routing and application support by searching for the optimum in high performance, low power consumption, composability, predictability, dependability and other general development requirements considered within SCALOPES. The purpose is to process protocol and/or payload data of NGN networks as a monitoring and data-processing unit.

The SCALOPES project will also answer the main issue in the design of a mobile terminal which is: "How can several types of user-oriented features be incorporated with seamless operation and evolution (including runtime adaptability), using minimum power resources for the required performance in dynamic SMT set-ups?"

VIDEO APPLICATION DOMAIN ~ In video surveillance applications, the aim is substantial improvement on actual commercial systems in three main areas: multi-standard image processing, independent of resolution, with high throughput and hard reliability requirements, image comprehension, like smart scene segmentation, behavioural tracking and complex measurements, and energy and cost-saving techniques, like triggering from external alerting sources and efficient communication handling. The stationary video application domain focuses on digital TV components and devices, on the one hand, and display controllers for multi-viewers, on the other. These display controllers for multi-viewers, i.e. large display walls, are part of complex networked visualisation systems, dealing with a huge amount of encoded video data complemented by metadata and monitoring information. These systems are traditionally resource and power-hungry, bulky equipment, statistically over-dimensioned to guarantee at run-time the necessary quality of service irrespective of the amount of data to be displayed. Solutions to make such systems embeddable are being investigated and are focusing on ways to reduce the amount of computing resources required locally by using the resources available through the network. ■

Dennis Alders
Coordinator of the SCALOPES project
NXP, the Netherlands, Central R&D

Dennis Alders received a M.Sc degree in Chemistry in 1992 from the University of Nijmegen (NL) and a PhD degree in Physics in 1996 from the University of Groningen (NL). He joined NXP (Philips) in 1998 to conduct research on efficient mapping of process networks on shared memory multiprocessor architectures. His research interests are in the design of embedded systems; high level modeling, hardware/software co-design, performance analyses, and source code transformation. He has 5 years of experience in European projects, and received in 2008 a silver achievement award for his work as a work package leader "for outstanding contributions to the ITEA program". Now he is in charge of the ARTEMIS-JU project SCALOPES which involves 39 key companies from 12 countries.

by Ad ten Berg ~ *ARTEMIS-IA Programme Coordinator*

GET READY FOR THE ARTEMIS-JU CALL 2010

Each year, ARTEMISIA Association organises a Brokerage Event to prepare the R&D community in Embedded Intelligence and Systems for the ARTEMIS-JU Calls. This event is designed to bring together a diverse mix of partners to exchange ideas for projects and to look for suitable partners. Some come with project ideas in need of partners, others come looking for a project in which they can contribute specific know-how. In an atmosphere of "creative chaos", these two poles find each other. One might say this is the place to be for meeting the right research partners for your consortium for the next ARTEMIS-JU Call, in just two days.

WELCOME ABOARD! ~ The Brokerage Event for the ARTEMIS-JU Call 2010, took place on 15 & 16 December 2009 and was, by all accounts, a success. With 240 people attending from 18 different countries, it was an increase of 25% on the previous event. Some were in search of a specific partner for an almost ready research idea and they succeeded already the first morning. Needless to say that such a proposal was not presented in plenary. However, evidently most of the proposals were presented after a hard day's collaboration. Of the more than 40 project ideas that were presented on the first day, about 21 project proposals resulted after two intensive days of meeting & matching.

FERTILE GROUND ~ Is the Brokerage Event fertile ground for submitting proposals in the ARTEMIS-JU programme? To find the answer, ARTEMIS Magazine asked the ARTEMIS-JU to investigate the result of the Brokerage project ideas in the ARTEMIS-JU Call 2009.

According to Alun Foster, Programme Manager of the ARTEMIS-JU Office: "The ARTEMIS Brokerage Event for Call 2009 yielded 28 ideas for ARTEMIS projects. Of these, 14 were directly traceable to project outlines submitted to the call and a further 4 projects were traceable to project outlines based on the brief description of their technical content. Others that also contained similarities were too tenuous to be sure of a structural link so were not included in this analysis. Of the 56 project outlines submitted to Call 2009, 18 can be considered as emanating directly from the preceding brokerage event (32%) and 15 of these went on to become one of the 44 full project proposals submitted to the call (34%). Seven of these were ranked above the selection threshold (47% of 'Brokerage' proposals and 29% of the 24 successful candidates) and six were retained for final negotiations (46% of the total 13 projects retained), being within the anticipated reach of the available national funding budgets".

HIGH SUCCESS RATE ~ Based on the rating as mentioned above, Eric Schutz, the Executive Director of the ARTEMIS Joint Undertaking, concluded that "of all the initial project outlines, about 1/3 come from the ARTEMIS Brokerage Event and 83% of these go on to become full project proposals. This is higher than the average for all POs (79%). This is evidence that those projects that passed through the brokerage event clearly have higher quality and increased chances of becoming funded."

While the brokerage, numerically, addresses about 1/3 of the active community in Embedded Systems who propose ARTEMIS projects, the apparent quality of the proposals that come out of ARTEMIS brokerage events is generally higher than average. In addition to the general benefits of networking at such event, the Brokerage Event could be considered as fertile ground and is really a head start in forming succesful consortia; it evidently increases your success in submitting proposals in the ARTEMIS-JU programme. On the next pages you will find three interviews of ARTEMISIA members who participated in Amsterdam. Let us take a closer reality check and see what their opinion is. ■

by Chris Horgan

INTERVIEW WITH DR. FABRIZIO AIROLDI

PERFORM A DOUBLE TASK

What kind of company is Akhela?
Akhela is the ICT company of Saras Group with particular responsibility for two main areas: the development and management of IT services and Embedded Systems. Our total revenues come to nearly 20 million euros annually and of the 225 employees, roughly 20% are dedicated to the embedded systems field. In planning and developing embedded systems, Akhela has built up substantial knowledge of real-time operating systems, signal processing and software development with key assignments in automotive, avionics, multimedia systems for consumer applications and telecommunication fields. We have created different applications particularly in the automotive field (our main business). We have a long tradition in powertrain systems and ECU where we have developed operating systems, algorithms for engine control, injections and ignitions drivers for gasoline, gas and diesel and also for reducing pollution and increasing engine performance and so on. More recently we have been involved in many projects related to HMI and infotainment systems, with and without open source.

Dr. Fabrizio Airoldi

Dr. Fabrizio Airoldi is director of the R&D division of Akhela. After graduation with a degree in Computer Science from Milan University, he spent some time in the silicon industry gaining significant experience and competence in the System-on-Chip field. Before heading up the R&D division, Fabrizio worked as Embedded Division Chief Technology Officer at Akhela. Not only does he have considerable experience in the management of large and medium-sized teams but he also has significant competences in embedded systems. He has also been an FP6 evaluator.

What experience does Akhela have with European Innovation Programmes and ARTEMIS projects?
While the R&D division of Akhela is very young, we have already booked some results. Our R&D team worked very hard in the 2009 on a European project, and we were able to present five FP7 projects, two of them as coordinator. Now, fingers crossed, we are working for the ARTEMIS call. Over the last year we have been studying how ARTEMIS works, and the projects that have been presented in past calls. This preliminary work enabled us to get the most of the recent brokerage event, increasing our network and actively participating in some consortiums, such as the very good consortium coordinated by University of Cagliari in the DISC project. As a fast-growing company which invests in research to boost its technological competences and identify new areas for development, we feel it is useful to participate in ARTEMIS projects.

We confess that the results of participation have been better than expected. In fact, Akhela competencies in embedded systems are very heterogeneous and we have able to contribute to a lot of projects. Our company think that the ARTEMIS technology platform is the right way to establish a European view of research for the embedded systems. And we also think that such technology platforms are a very interesting 'tool' for the European researchers.

HOW DO YOU APPROACH MATCHMAKING AND CREATING A CONSORTIUM? ~ Because we were looking to chose projects close to our business or that we want to develop in the future, we feel there must be a good balance between academic, development and end-user partners. However, the most important thing is that the partners are keen to actively work on the project from the beginning and that there is good synergy among them. We can play two different roles in the consortium: developer and end user. On the one hand, Akhela embedded division is able to develop embedded software and to specify the research activity in this field, on the other, Akhela is owned by a big refinery and we can propose some industrial case studies for new technologies. During the brokerage we encountered some groups with both needs, and so we hope to perform a double task. Presently we are participating in several consortiums, so we are defining the final team and working on writing the proposal. We did note during the Brokerage Event that while academic partners were well represented, SMEs and large enterprises were less present. For the strength of the projects we would like to have in our consortium some other companies that can implement or do the experimentation of the new technologies.

And your participation ambitions?
We want to have two or three project outlines. In particular, one project related to safety certification for the automotive field and one related to the safety and security approach for industrial plants like our refinery. In fact, we are focusing on both. Of course, our real wish is that all the good ideas proposed during the event get approved! ■

by Chris Horgan

INTERVIEW WITH ARUN JUNAI

HIGH DEGREE OF PRAGMATISM AND PRACTICALITY

Arun Junai works in the TNO Science and Industry as coordinator for EU research programmes. His work consists largely of lobbying and matchmaking for FP7 and JTI calls and projects. Arun is originally a materials scientist and joined TNO in 1992 where he began as a senior consultant and moved on to become a departmental head before taking on his current role in the European programme scene. Embedded system is one of the research fields of TNO.

What kind of company is TNO? **~** TNO is an independent research organisation whose expertise and research helps create new products that make life more amenable and valuable and help companies to innovate. We work for a variety of customers, nationally and internationally: governments, the SME sector, large companies, service providers and non-governmental organisations. As 'knowledge brokers' we advise our customers, moreover, on finding optimum solutions that are geared precisely to the questions they have. In 2008 total consolidated turnover was 600 million euros, a third of which was government funding for the development of new knowledge. The market turnover of 405 million euros comprises 318 million euros from the contract assignments of our five core areas (Quality of Life, Defence, Security and Safety, Science and Industry, Built Environment and Geosciences, and Information and Communication Technology) and the other 93 million euros was earned by the knowledge commercialised or conducted through some 55 companies operating under TNO Companies BV. TNO employs around 4500 people.

What experience does TNO have with European Innovation Programmes and ARTEMIS-JU projects? **~** TNO has been active for many years in EU framework programmes, throughout the whole trajectory from calls to tender, proposal to negotiations, execution and close. With a success rate of 30% on thirty proposals in the FP7 round, this means 10 or so projects annually for TNO Science and Industry. Currently we are involved in 25 running projects. We coordinate around 10% of all the projects in which we are involved. There is a clear distinction to be made between the EU FP projects, which are on a pre-competitive, applied research basis, and industry-driven JTIs and the newer PPPs, or public-private partnerships, where the focus lies on industrial applications and an approach characterised by a high degree of pragmatism and practicality. In respect of embedded systems, TNO Science and Industry involvement centres on five key research themes, with an average of 60 people per research team. These themes are high-end equipment, automotive, health, space and sciences, and space applications. In terms of the ARTEMIS experience, TNO is a newcomer. But the prospects are very interesting. TNO is very active in the European Technology Platforms (ETPs) in Europe, linking manufacturing to other platforms. This both encourages and demands considerable networking and sharing. ARTEMISIA facilitate the knowledge development and sharing through consortium creation.

How do you approach matchmaking and creating a consortium? **~** When we look at the subject of matchmaking and consortium building, we review the entire knowledge chain and ask relevant questions, such as who can provide the required technology and who are the problem holders? How can we effect the translation into industrial solutions, or products? And, of course, an essential aspect, who are the communication providers? You can draw up lists and lists of requirements and wishes and match up supply and demand very precisely but when it comes down to it, nothing beats face-to-face contact. And that's where a brokerage event, such as the one in Amsterdam, has real value. It is a meeting place where people can get together, swap ideas and suggestions, put a face to a name and build the kinds of network so vital to shaping the technology development of the future. As for consortium-building, I would say that our preference is for the consortium to be industry led – it keeps the focus sharply on the end target. And as for the partners we are looking for, these are mainly from industry.

And your participation ambitions? **~** We are very keen on participation. TNO is a contract research organisation whose mission is to boost the capacity of industry and government to compete and innovate, so the development of knowledge is a crucial component of this mission. Participation seems to be a win-win situation – we have a lot to offer and we can benefit greatly from the knowledge sharing that ARTEMIS promotes. ■

by Chris Horgan

INTERVIEW WITH ROBERTO ZAFALON

WANTED! SMES AND PARTNERS FROM EASTERN EUROPE

Venetian-born Roberto Zafalon is STMicroelectronics' EU Projects Director in Italy, charged with fostering and leveraging the link between ST technology groups and the R&D cooperative EU programmes. Roberto has been with STMicroelectronics for 20 years. Since July 2007, he has been focusing on the vision and roadmap, seeking project financing and driving industrial R&D teams to pursue innovative solutions in the field of embedded systems and nanolectronics, for corporate product divisions and labs. He has significant experience of managing and coordinating industrial and geographically distributed R&D teams as well as managing resources and international research projects, including European MEDEA+ and FP5, FP6 and FP7 research frameworks. He is member of the international committee currently responsible for defining the next 2007-2012 European industrial Technology Platform's programme and strategic research agenda for Nanotechnology (ENIAC) and Embedded Systems (ARTEMIS).

What kind of company is ST? ~ STMicroelectronics is the world's fifth largest semiconductor company with net revenues of USD 9.84 billion in 2008 and a workforce of around 50,000 people worldwide. The company's sales are well balanced between the semiconductor industry's five major high-growth sectors: Communications (36%), Consumer (17%), Computer (16%), Automotive (15%) and Industrial (17%). ST is the leading producer of application-specific analog chips and power conversion devices as well as the premier supplier of semiconductors for the industrial market, set-top box applications, and MEMS (micro-electromechanical systems) chips for portable and consumer devices, including game controllers and smart phones. In the mobile phone market, ST and Ericsson joined forced to establish a new company STEricsson to take mobile solutions for cell phones through to the fourth generation. Furthermore, ST is the world's ranked third ranked supplier of automotive integrated circuits and of chips for computer peripherals, and fifth in the rapidly expanding market for MEMS. A chief focal area is real-time critical platforms for the automotive industry in which smart services and embedded computing are geared towards high-priority issues like energy efficiency and renewable energy. In other words, 'smart green' energy transportation and supply.

What experience does ST have with European Innovation Programmes and Artemis projects? ~ ST could be considered a player of some considerable experience, with a high degree of activity in FP6 and FP7 programmes targeting nanomaterials, energy and transportation. In fact, ST was one of the founding fathers of nanoelectronics and silicon chip integration. In FP7 ST has been involved in both large and medium-sized ICT projects, often in a coordinating role, with specific topics being future-geared automotive, embedded systems and control systems. Other participation has been in what might be termed 'high-momentum' topics, such as improving the quality of wellness and healthcare so that it can be affordable. As for Artemis, ST has been involved in Call 1 and Call 2 projects but not in any coordinating role yet. In the application domains, ST acts as a technology provider for electronics, drivers, software and operating systems.

What did you think of the Amsterdam Brokerage Event? ~ We perceived it as a key strategic trigger, with a lot of positives. The organisation was very well managed and the opportunity to share project ideas, visions and future projections was excellent. With around 300 or so representatives, there was also plenty of opportunity for contacts to be laid. The posters were very effective. However, there were some problems in the practical logistics of such an event – unavoidable really but maybe something to be considered for next time. Parallel sessions do not facilitate sharing, despite the option of a summarising plenary session.

How do you approach matchmaking and creating a consortium? ~ When creating a consortium, for instance, in the safety-critical and automotive areas, we need to look at the whole supply chain so that the consortium reflects or is represented by the entire chain in its composition and input. And when we look at the matchmaking criteria in forming such a consortium we look certainly to research centres and universities since these are part of the research networks that we regard as essential. We distinguish two types of consortium: the JTIs (joint technology initiatives) tend to be industry driven whereas the FP7 is more geared to the research component.

And your participation ambitions? ~ In respect of Call 3 project outlines, we are looking for more participation by SMEs and partners from Eastern Europe to complete the consortia that will have to meet the requirements. ■

ARTEMIS JU aims to help European industry consolidate and reinforce its world leadership in embedded computing technologies. The economic impact in terms of jobs and growth is expected to exceed €100 billion over ten years. The European Union recognises the strategic importance of Embedded Computing Systems and launched the ARTEMIS Joint Technology Initiative (JTI). The ARTEMIS JTI is implemented as a Joint Undertaking (JU) which is a public-private partnership between:

> The European Commission
> Participating Member and Associated States, by now 22 countries
> ARTEMISIA, the non-profit Industrial Association of R&D actors in the field of ARTEMIS

The ARTEMIS JU will manage and coordinate research activities through open calls for proposals through a ten-year, €2.7 billion research programme on Embedded Computing Systems. The programme is open to organisations in European Union member states and associated countries. Selected projects will be co-financed by the Joint Undertaking and the member states that have joined ARTEMIS. The ARTEMIS JU will implement significant parts of the ARTEMIS–ETP Strategic Research Agenda co-funded by industry, research organisations, member states and the Commission's own ICT programme. The third ARTEMIS Call was launched on 26 February 2010.

ARTEMIS JOINT UNDERTAKING AWARDED AUTONOMY STATUS UNDER THE LEADERSHIP OF ERIC SCHUTZ, EXECUTIVE DIRECTOR

As reported in ARTEMIS Magazine 5, the ARTEMIS-JU Office was established in September 2009 in Brussels. In that interview, Eric Schutz, the new Executive Director of the ARTEMIS Joint Undertaking, stated that it was his top priority to achieve autonomy for the JU Office. We can now say that he has had an auspicious start to his tenure since 1 September 2009, with the status of autonomous Community Body being granted by the European Commission on 26 October 2009. This is an important milestone in the short history of Joint Technology Initiatives. The Executive Director has to serve as the link between all the stakeholders - the European Commission, the participating member and associated states, and ARTEMISIA, the industry association of R&D actors in the field of ARTEMIS.

A FIRST ~ The ARTEMIS Joint Undertaking will run till 2017, with the cost of the research activities within the initiative totalling up to €2.7 billion. Its aim is to implement the Joint Technology Initiative on Embedded Systems and Intelligence. Eric Schutz explains: "The ARTEMIS JU Office executes the programme from the publication of calls through evaluation and contract negotiation, coordination with national funding authorities, project follow-up and reviews through to the delivery of the final payment. The JU office exists to serve the ARTEMIS community of stakeholders, which means there will be constant communication between the JU Office and all the partners, including the Commission, the ARTEMIS member states and ARTEMISIA. Having to be independent as Executive Director, it was vital for me to get the ARTEMIS JU declared autonomous as quickly as possible. I am very happy that we have been able to work in this way since 26 October. You can imagine how honoured I am to be the Executive Director of the first autonomous JU."

Accountable to the Governing Board of the ARTEMIS Joint Undertaking, Eric Schutz will ensure that the initiative's mission and objectives are achieved. His responsibilities include the efficient organisation of the calls for proposals, the evaluation of submitted proposals, the negotiation and conclusion of grant agreements as well as their subsequent monitoring and finalisation.

IMPORTANT MILESTONE ~ Klaus Grimm, President of the ARTEMISIA Association and Chairman of the ARTEMIS Governing Board welcomes the autonomous status of the ARTEMIS-JU Office, saying: "We fully agree that the position of this office needs to be neutral and therefore autonomous to shelter all the stakeholders in the ARTEMIS Joint Undertaking." Thierry Van der Pyl, and Aldo Covello, the former and the current Chair of the Public Authorities Board of the ARTEMIS JU underline that as well: "This is an important milestone for the ARTEMIS Joint Undertaking. It demonstrates that, thanks to the combined efforts of all parties and of the Commission in particular, we have successfully delivered the very first autonomous R&D public-private partnership to the research community, member states and the community as a single instrument with common objectives. All parties will have to stand by their commitments and play their roles constructively if the ambitious goals of the ARTEMIS Joint Undertaking are to be achieved ■

CALL 2010 IN THE STARTING BLOCKS

Call 2009 is hardly behind us and Call 2010 is already tearing at the leash to go. As I write this, Project Coordinators from the successfully negotiated Call 2009 projects are making their way to the ARTEMIS JU Office in Brussels to get the low-down on how best to get their projects up and running smoothly, while the Programme team here is already busy preparing for the Call 2010 launch, so there's a lot going on.

Call 2010 will, in many respects, be a carbon copy of Call 2009 but with a few subtle changes. Changes that, we hope, will help us manage the increasing number of ARTEMIS projects smoothly and efficiently so that we can continue to offer the high level of support to the projects that we strive to achieve. First, some hard data.

The Call will, as in 2009, be a two-step one, with "PO" and "FPP" phases and will open on February 26th in the morning. The work programme for this call was proposed by ARTEMISIA and has already been accepted by the Public Authorities Board, and can be consulted on-line. Project proposers can then submit a Project Outline (PO - a short description of the project, including basic data about the resources needed) any time before March 26th at 17h00:00.000. As ever, this deadline is extremely strict so, as we expect quite a large number of proposals, it will be extremely unwise to wait until the last minute to submit (we recommend aiming to submit a week before this deadline, so that the proposal is definitely in, leaving time for any last-minute fine-tuning).

ELECTRONIC PROPOSAL SUBMISSION SYSTEM ~ To submit proposals, we will be using the FP7 "Electronic Proposal Submission System" EPSS. For the users, there's no significant difference, except that people who may already have submitted proposals to FP7 can make use of the "PIC" system, so that their previously submitted information can be recovered simply and quickly. The EPSS also allows us, at the JU side, to integrate the project information into the rest of the FP7 project management tool chain we use, which will help in the later support of the projects. We are working on providing even more extensive support documentation for proposers, too, which will be available as soon as the Call opens.

PROJECT OUTLINES ~ The Project Outlines will be reviewed by external experts, as well as the National Funding Authorities, and feedback will be given about the proposal. This is not an acceptance gate! Even though the PO phase is mandatory, the feedback is designed to let proposers improve the quality of their proposal, and how it fits in with the ARTEMIS programme and any specific eligibility criteria there may be locally. A project cannot 'fail' the PO phase as such, though it would be very unwise to ignore the feedback while completing the Full Project Proposal (FPP)!

FULL PROJECT PROPOSALS ~ The FPP deadline is 1 September 2010 at 17h00:00.000 (again, a very strict deadline - don't miss it!). Yes, I know, it's a painful date, but we need to keep this if we are to get all the proposals evaluated and the successful ones negotiated, in time to let the projects start early in 2011. The EPSS will be used for this phase, too, which will minimise the amount of repeated data proposers will need to enter.

At that time, dare I say it, we'll already be looking forward to Call 2011!

By Alun Foster ~ *Programme Manager ARTEMIS-JU*

CALL 2010
KEY DATES

> CALL PUBLICATION: 26 FEBRUARY 2010

> DEADLINE FOR PROJECT OUTLINES: 26 MARCH 2010
- Formal feedback ~ end May

> DEADLINE FOR FULL PROJECT PROPOSALS: 1 SEPTEMBER 2010
- Formal feedback end October
- Negotiations completed by end December

> PROJECTS CAN START EARLY 2011

by Alun Foster ~ *Programme Manager ARTEMIS-JU*

ARTEMIS-JU CALL 2009:

13 SELECTED PROJECTS!

This Call, executed in the transition phase of being operated by the Commission then by the (now) autonomous JU staff, has produced another collection of good ARTEMIS projects, to join those from the first Call.

Call 2009 was the first to operate in a two-phase mode. A Project Outline (PO) phase yielded 56 proposals which were reviewed and feedback given to the proposers (the PO phase is non-gating, but mandatory). For the FPP phase, 44 proposals were received on 3/9/2009 and evaluations completed on 2/10/2009. (During this phase, the handover from the Commission staff to the JU staff was completed). The Mandate to negotiate the scored projects was finalised in the PAB meeting of 22/10/2009, with 13 projects retained for negotiation, 6 projects on a Reserve List, 5 projects not feasible financially though above the minimum score threshold. 20 projects were informed that they were below the selection threshold.

On December 15th (the end of negotiation mandate), 11 projects had successfully completed negotiations, while another 3 projects were granted temporary extension of the mandate. Of these three, two became merged and, just prior to the PAB and GB meeting of 28th January 2010, a total of 13 projects had successfully been negotiated. This table summarise each project's technical objectives.

1

ACROSS

Project duration (months): 36
Start date: 01/04/2010
Total Costs: 16.1 M€

ACROSS will develop and implement an ARTEMIS cross-domain architecture for embedded Multi-Processor SoCs based on the architecture blueprint developed in the FP7 project GENESYS (Generic Embedded System Architecture), and develop a first generic MPSoC implementation in an FPGA. The ACROSS MPSoC will provide a stable set of core services as a foundation for the component-based development of embedded systems with short-time-to-market, low cost and high dependability. The ACROSS-MPSoC will be a universal platform for automotive, aerospace and industrial control systems in order to realise the benefits of the economies of scale of the semiconductor technology. The benefits of the cross-domain architecture will be shown in demonstrators from the targeted application domains.

3

ASAM

Project duration (months): 36
Start date: 01/04/2010
Total Costs: 5.83 M€

ASAM addresses a uniform process of automatic architecture synthesis and application mapping for heterogeneous, multi-processor embedded systems, defining a new and unified design methodology, as well as related synthesis and prototyping tool-chains. For this, a highly efficient automatic synthesis flow will be created from the algorithmic specification down to its hardware/software implementation at the circuit/code level. The automatic synthesis flow will let the system and algorithm designers focus on the higher-level development issues, relieving them from the lower-level implementation concerns. In this way, the new design environment will allow rapid exploration of the high-level and algorithm design space and, consequently, quick development of high-quality designs.

4

CHIRON

Project duration (months): 36
Start date: 01/03/2010
Total Costs: 18.1 M€

Addressing growing health-care concerns, CHIRON will combine state-of-the art technologies and innovative solutions into an integrated framework designed for an effective and person-centric health management over the complete care cycle. It will address and harmonize the needs of all the three main beneficiaries of the healthcare process, i.e., the patients using the services, the medical professionals and the whole community, putting the citizens at the core of the whole healthcare cycle by considering them as "persons" with specificities and identities, empowering them to manage their own health. CHIRON will enlarge the boundaries of healthcare by fostering a seamless integration of clinical, at home and mobile settings, in a concept of a "continuum of care", with a focus on moving from treatment to prevention. By developing a reference-architecture for personal healthcare, CHIRON will ensure the interoperability between heterogeneous devices and services, offer reliable and secure patient data management and a seamless integration with the clinical workflow. The CHIRON system will provide powerful supporting ICT tools and at the same time it will ensure that the patients and the doctors remain the protagonists of the healthcare process that has been designed around them.

5

eSONIA

Project duration (months): 36
Start date: 01/01/2010
Total Costs: 12.1 M€

In Europe, manufacturing represents approximately 22% of GDP, and it is estimated that 75% of GDP and 70% of employment is related to manufacturing. The direct cost of maintenance is equivalent to 4% to 8% of the total sales turnover and, depending on the industry, maintenance costs can represent between 15% and 60% of production cost. However, today, factory's operating conditions cannot be comprehensively monitored, since there is no infrastructure for holistic and continuous measurement and visualisation of relevant information.
This lack of insight prevents efficient decision making in real-time (e.g. recovery from undesired situations), reducing efficiency and increasing maintenance costs and safety risks. For example, the following figures demand improvement: 70% of industrial accidents are caused by human errors during complex operations, and 5% of all fatal work accidents in Spain in 2007 took place during the carrying out of maintenance-related activities. In addition, several studies have indicated that a significant increase in Overall Equipment Effectiveness (OEE), (from today's 60% to 75%), entailing important profit improvements, is achievable through maintenance improvements by using new technology, modern high-tech equipment and better planning.
eSONIA will realise the asset-aware and self-recovering plant through pervasive, heterogeneous (wireline and wireless) IPv6-based embedded devices with on-board specialised services, glued together by middleware capitalising on the service oriented approach. All of this will be used for the first time in industry to support continuous monitoring, diagnostics, prognostics and control of assets, regardless of their physical location. The data gathered allow efficient automatic maintenance schedules and improved operator dispatch and repair performance.
eSONIA means greater predictability of plant behaviour and visibility, reduced safety risks, enhanced security and cost efficiency.

5

iFEST

Project duration (months): 36
Start date: 01/04/2010
Total Costs: 15.8 M€

iFEST will specify and develop an integration framework for establishing and maintaining tool chains for the engineering of complex industrial embedded systems. Specific emphasis is placed on open tool chains for HW/SW co-design of heterogeneous and multi-core solutions, and life cycle support for an expected operational life time of several decades.
iFEST results will demonstrate a potential reduction by 20% of both time-to-market and engineering lifecycle costs, including cost of poor quality. It will enable engineers to explore the architectural design space at a high level of abstraction, select a cost effective design, and from the abstract models produce, semi-automatically, the hardware

and software implementations in a cost effective balance. A major innovation in this respect is the targeted integration of tools from the world of model driven engineering with traditional HW/SW co-design tools.

Several iFEST industrial case studies will validate the integration framework and two tool chains, for control and streaming applications. The integration framework will permit tools to be readily replaced within the tool chain; thus dealing with issues such as tool obsolescence and tool lock-in.
iFEST will promote standardisation of project results to encourage industrial up-take, aligned with the ARTEMISIA Working Groups on standardisation and tool platforms. It will bring the industry from a state where efficient tool usage in practice is low, to a state where innovative products and services can be designed much more efficiently due to well-functioning tool chains. Having a greatly improved design capacity will create new markets and redefine existing ones for industrial embedded systems.

6

ME3GAS

Project duration (months): 12
Start date: 01/04/2010
Total Costs: 15.7 M€

Put consumers in control of their appliances to let them effortlessly optimise energy efficiency usage without compromising comfort or convenience. This is the goal of ME^{3}Gas: specifically to addresses reduction in energy usage and CO2 footprint in households and commercial buildings. The use of Embedded Intelligence is what makes energy smart, and is the heart of energy-efficient technologies. ME^{3}Gas will make use of the service-oriented middleware for embedded systems being developed in the Hydra project and use its huge potential to create services and applications across heterogeneous devices, to develop an energy-aware middleware platform.
But ME^{3}Gas can only have commercial and residential relevance if it can be used to save energy in real-world applications. To demonstrate this, it includes a critical step of retrofit installation of the developed hardware and GUI platforms into real applications. In this context, ME^{3}Gas will develop a new generation of smart gas meters, based on embedded electronics, communications and the remote management of a shut-off valve, which will offer a whole range of intelligent features: management of multiple tariffs and payment modalities, remote gas cut off, security alarms, etc.

ME^{3}Gas will also contribute to the standardization work being carried out currently in Europe in the smart metering field (under the M/441 mandate of the EC mainly). The work will propose a standard for a European Gas Metering Infrastructure, which can be a part of a multi-utility platform to be made within the project.

7

POLLUX

Project duration (months): 36
Start date: 01/03/2010
Total Costs: 33.3 M€

POLLUX will develop a distributed real time ES platform for next generation electric vehicles, by using a component and programming-based design methodology. Reference designs and ES architectures for high efficiency innovative mechatronics systems will be addressed, focusing on composability, networking, security, robustness, diagnosis, maintenance, integrated resource management, evolvability and self-organisation.
Next generation EVs will begin the convergence between computer and automotive architectures: future cars will be mechatronic systems comprising a multitude of plug-and-play and self configurable peripherals. Peripherals will be embedded systems containing hardware, algorithms, software. The architecture will be based on distributed energy while the propulsion systems will adopt radical new control concepts. Sensing, actuation, signal processing and computing devices will be embedded in the electronic equipment, electrical motors, batteries and the mechanical parts as well.
The systems used to control the chassis and the power train will form the "computing engine" that automates lower level tasks during vehicle use (driver assistance, terrain evaluation, predictive battery management) and will enable future higher level functionalities (auto pilot), by means of novel user interfaces.
POLLUX is synergetic with the ENIAC E3Car project which will develop nanoelectronics technologies, devices, circuits, and modules for EVs in preparation for the launch of a massive European EV market by 2015-2020.

8

R3-COP

Project duration (months): 36
Start date: 01/03/2010
Total Costs: 18.3 M€

Safe and robust autonomous systems are one of the – if not the – most important instantiation of embedded systems in mid-term future, simply because the application domains are so diverse, from transportation over manufacturing to farming, surveillance (indoor, land, air, and sea) to care as well as entertainment. Consequently, the ARTEMIS Strategy Group identified "Autonomous Systems" as one of the targets of the next ARTEMIS SRA. However, today, a large number of different approaches and platforms exist, rendering an economic realisation of such systems currently unrealistic (except in the manufacturing domain, where robots are already industrially exploited). Simultaneously, as such systems increasingly share space – and even closely cooperate – with humans, there is an urgent need for providing every possible means and measures to assert and guarantee

their dependability, in particular safety and robustness. R3-COP will progress autonomous systems in two directions: technology and methodology.
Technology: R3-COP will develop a fault-tolerant high-performance processing platform, based on a multi-core architecture, as well as innovative system components for robust perception of the environment including sensor fusion, and for reasoning and reliable action control. Methodology: a methodology-based development framework will enable economic development of reference platforms for various robotic applications as well as dedicated solutions. A tool platform will allow for guarded application of the design methodology, including new test strategies and tools. The outcomes will be applied in a series of demonstrators from ground-based (medical and domestic), airborne and underwater domains.

9

RECOMP

Project duration (months): 36
Start date: 01/04/2010
Total Costs: 25.8 M€

RECOMP will establish methods, tools and platforms for enabling cost-efficient (re-)certification of safety-critical and mixed-criticality systems. Applications addressed are automotive, aerospace, industrial control systems, and lifts and transportation systems.
RECOMP recognises the fact that the increasing processing power of embedded systems is mainly provided by increasing the number of processing cores. The increased numbers of cores is a design challenge in the safety-critical area, as there are no established approaches to achieve certification. At the same time there is an increased need for flexibility in the products in the safety-critical market. This need for flexibility puts new requirements on the customization and the upgradability of both the non-safety-critical and safety-critical parts. The difficulty with this is the large cost in both effort and money of the re-certification of the modified software.
RECOMP will provide reference designs and platform architectures, together with the required design methods and tools, for achieving cost-effective certification and re-certification of mixed-criticality, component based, multicore systems. The aim of RECOMP is to define a European standard reference technology, supported by the European tool vendors participating in RECOMP.

10

p.S.HI.E.L.D.

Project duration (months): 12
Start date: 1/03/2010
Total Costs: 5.4 M€

This Project is a pilot version (hence: "p.S.HI.E.L.D") of the S.HI.E.L.D. project. The pilot is foreseen to be a pioneer investigation, to be enhanced with R&D activities that will be proposed in the future ARTEMIS Calls.

SHIELD aims at addressing Security, Privacy and Dependability (SPD) in the context of Embedded Systems (ESs) as "built in" rather than as "add-on" functionalities, proposing and perceiving the first step toward SPD certification for future ES.
The leading concept is to demonstrate composability of SPD technologies. Starting from current SPD solutions in ESs, the project will develop new technologies and consolidate the available ones in a solid basis that will become the reference for a new generation of "SPD-ready" ESs. The composability of the SHIELD architectural framework will have great impact on system design cost and time to market of new SPD solutions. At the same time, the integrated use of SPD metrics will have impact on the qualification, (re-) certification and (re-) validation process, making them faster, easier and more widely accepted.

11

SIMPLE

Project duration (months): 36
Start date: 01/09/2010
Total Costs: 7.43 M€

The main goal of SIMPLE is to research and deliver an intelligent, self-organising embedded middleware platform, designed for the integration of manufacturing and logistics. SIMPLE will address the self-organisation and cooperation of wireless sensors and smart (RFID) tags for federated, open and trusted use in the manufacturing and logistics applications.
The primary idea is to enable the dynamic interworking of ultra heterogeneous sensors and tags, which should autonomously organise in hierarchies, thus leveraging the development of a new class of secure, scalable, cost-effective, and easy-to-deploy "smart factory" and logistics applications. The SIMPLE outcomes aim at compensating the current lack of solutions capable of monitoring the state of shipments at different grouping levels (e.g., at the crate and case levels) and, more generally, of tracing goods along the whole supply chain. SIMPLE will prototype, test and validate the technologies using two test-beds under normal operation: - a complete manufacturing plant solution, and a complete logistics supply chain.

12

SMARCOS

Project duration (months): 36
Start date: 01/01/2010
Total Costs: 13.5 M€

SMARCOS helps users of interconnected embedded systems by ensuring their inter-usability. Many products today connect with web services

(media players, refrigerators, e-books, even cars). This distributed computing is becoming the norm in embedded systems, but connection problems, firmware incompatibilities, incomprehensible dialogue boxes and just plain bugs plague many commercial offerings. New challenges have also come up for user interaction.
Existing efforts towards interoperability (e.g. ARTEMIS project SOFIA) have largely focused on architectures. We extend these efforts on the user level. SMARCOS allows devices and services to communicate in UI level terms and symbols, exchange context information, user actions, and semantic data. It allows applications to follow the user's actions, predict needs, and react appropriately to unexpected actions. SMARCOS plans several pilots that implement the use cases, including one large trial in a major public event (2012 London Olympics). Along the project, several smaller prototypes will be implemented.

13

SMECY

Project duration (months): 36
Start date: 01/02/2010
Total Costs: 20.5 M€

SMECY envisions that recently emerged multi-core technologies will rapidly develop to massively parallel computing environments which, due to improved performance, energy and cost properties, will extensively penetrate the embedded system industry in a few years. This will affect and shape the whole business landscape, e.g. semiconductor vendors need to be capable of offering advanced multi-core platforms to diverse application sectors, Intellectual Property (IP) providers need to re-target existing and develop new solutions to be compatible with evolving multi-core platforms and the need of embedded system houses, in addition to product architecture adaptations and renewing their system, architecture, software and hardware development processes. The mission of SMECY is to develop new programming technologies enabling the exploitation of many (100s) core architectures. The goal of this ARTEMIS project is to launch an ambitious European initiative to match initiatives in Asia (e.g. teams funded by JST/CREST programmes) and USA (e.g. PARLAB in Berkeley, Parallel@illinois and Pervasive Parallelism Laboratory in Stanford) and to enable Europe to become the leader. ■

CALL 2008 PROJECTS STATUS

The twelve pristine ARTEMIS projects that were successfully negotiated at the end of 2008 all left the starting blocks pretty well on time. Sadly, as with any complex machine, unexpected hurdles can pop up the first time you try to use it, and this proved to be the case in certain participating countries from our first Call. While many projects were able to keep running unhindered, a few had to slow down and wait for some blocking issues to be cleared out of the way.

But, where there's a will there's a way, and there was certainly no shortage of good will and a good deal of creative thinking on the part of the national representatives and of the European Commission Project Officers in charge of operating the first Call. Thanks to them, some very pragmatic and practicable solutions were found and pressed into play as quickly as possible, taking into account, of course, the inevitable legalities involved (it's tax-payers' money, after all).

As a result, and after some internal reconfiguration of some of the projects and their coordinators, all of the Call 2008 projects are now up and running although a few inevitably lag behind their originally planned schedules.

With work now progressing on many fronts, some partners have called me to ask about their JU funding, which they had not yet received even though their national authority was up to speed with the paperwork. The handover from the Commission to the JU staff, when the JU became autonomous in October 2009, happened remarkably smoothly, so the problem couldn't really be there. It turned out that, for some projects, the JU Grant Agreement had not, or had only recently, actually "come into force". Once the project coordinator and the JU have signed the Grant Agreement, all of the other project partners need to sign a so-called "accession form" to this contract to say that they agree to it (it's simpler that way).

In order to be valid, the JU Grant Agreement must involve three different partners in at least three different countries, so the JU must receive at least two accession forms, in addition to the signed agreement, since without them, the Grant Agreement is not 'in force' and no payment of any sort may be made. In the meantime, a considerable log jam of payment requests had built up.
However, now that the accession form issue has, for the large part, been resolved, payments are starting to flow. It's a good tip for Call 2009 coordinators, therefore, to make sure that all the partners get their paperwork in order as soon as they can!

2010 will be the year in which many of the projects – those that have not already done so – will be able to show off their interim results in their first Project Review meetings. These have been tentatively planned up to the May timeframe, and I'm really looking forward to seeing what they have achieved so far. ■

by Alun Foster ~ *Programme manager ARTEMIS-JU*

Editorial information

ARTEMIS Magazine is published 3 times a year by ARTEMIS-IA and ARTEMIS-JU.

ARTEMIS-IA is the Industry Association for R&D actors in the field of Advanced Research and Technology for EMbedded Intelligence and Systems. ARTEMIS-IA continues the work of the ARTEMIS European Platform in Embedded Systems and is since 2007 an association with about 185 members under Dutch law. ARTEMIS-IA creates the meeting place where key industry players and other R&D actors identify topics for major R&D projects that they want to pursue together, form consortia and initiate project proposals for joint collaboration, and building of ecosystems for Embedded Intelligence. ARTEMIS-IA is a founding member of the ARTEMIS Joint Undertaking (JU) which was established in 2008. The objective of the ARTEMIS-JU is to define and implement a Research Agenda for Embedded Computing Systems. It aims to help European industry consolidate and reinforce its world leadership in embedded computing technologies.

ARTEMIS-JU is a Public Private Partnership with the EC and participating member states. ARTEMISIA association is the private partner in the ARTEMIS-JU and represents its members towards the EC and member states. The ARTEMIS JU will manage and co-ordinate research activities through open calls for proposals through a 10-year, €2.5 billion research programme on Embedded Computing Systems.

ARTEMIS Magazine provides information on the developments within the ARTEMIS Technology Platform (ARTEMIS-IA) and in the ARTEMIS-JU. Its aim is to keep the ARTEMIS community and beyond updated about the Association, Joint Undertaking, programme status & progress, achievements and events in the field of ARTEMIS. An online version of ARTEMIS Magazine is available on www.artemisia-association.eu and www.artemis-ju.eu

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ARTEMIS news or events linked to the ARTEMIS programme,
its projects or general ARTEMIS related subjects.
Please submit your information to:
communications@artemisia-association.eu

by Ad ten Berg ~ *ARTEMIS-IA Programme Coordinator*

ARTEMISIA SUMMER CAMP 2010

As in previous years, ARTEMISIA intends to organise its annual "Summer Camp" in 2010, too. As you may already know, the summer camp is a privileged two-day gathering where ARTEMISIA members are invited to share their views as well as bring up new innovative and exciting topics in order to influence and update the development of the ARTEMIS programme. With its task to elaborate the Strategic Research Agenda (SRA) and propose the Multi-Annual Strategic Plan and its corresponding research agenda to the ARTEMIS JU, ARTEMISIA has conceived the summer camp as an efficient means to get the members to actively participate in the elaboration of these documents.

SUMMER SWOT ~ ARTEMISIA can look back on a very successful series of summer camps over the years. Important improvements that have been achieved include the development of the technical content of the eight sub-programmes as well as the concept of "Innovation Ecosystems" and "Centres of Innovation Excellence" as the kernel for the ARTEMIS strategy described in the Multi-Annual Strategic Plan. In 2009, all participants contributed to a multi-viewpoint analysis of the Strengths, Weaknesses, Opportunities and Threats (SWOT) of the 2006 version of the SRA. This SWOT analysis was the kick-off for the recalibration process of the SRA that will lead to a new version of the SRA in 2010.

In the 2010 summer camp, ARTEMISIA members will again have the opportunity to have their say in the annual cycle of "renewal" by proposing ideas to the ARTEMISIA community on new potential sub-programmes or other new work on innovations. The summer camp is an ARTEMISIA members-only event but capacity is limited please reserve your place early if you want to be sure of participating! Most likely the summer camp will be planned for the second week of June. For the latest information, please follow the announcements by e-mail and on the ARTEMISIA website. ■

Calendar

1 MARCH, 2010
NUREMBERG, GERMANY
ARTEMIS-JU CALL 2010
Information event (information: www.artemis-ju.eu)

2-3 MARCH, 2010
NUREMBERG, GERMANY
ARTEMIS SPRING EVENT
Information: www.artemisia-association.eu

2 - 4 MARCH, 2010
NUREMBERG, GERMANY
EMBEDDED WORLD 2010
Presenting the leading European event for the Embedded Community covering all areas of Embedded System development. In addition to hardware, software and tools, the conference will also be devoting itself to themes such as green electronics or project management and thus picking up current trends and developments.
More information: www.embedded-world.de

5 MARCH, 2010
ROME, ITALY
ARTEMIS-JU CALL 2010
Information day (for details see ARTEMISIA website)

9 MARCH, 2010
PARIS, FRANCE
ARTEMIS-JU CALL 2010
Information day (for details see ARTEMISIA website)

9 EN 10 JUNE, 2010
LOCATION TO BE DETERMINED
ARTEMIS SUMMER CAMP
More information: www.artemisia-association.eu

27 - 29 SEPTEMBER 2010
BRUSSELS, BELGIUM
ICT 2010
This biennial event has become a unique gathering point for researchers, business people, investors, and high level policy makers in the field of digital innovation. ICT 2010 will focus on policy priorities such as Europe's Digital Agenda and the next financial programme of the European Union for funding research and innovation in ICT.
More information: http://ec.europa.eu/information_society/events/ict/2010/index_en.htm

26 - 27 OCTOBER 2010
Ghent, Belgium
ARTEMIS AUTUMN EVENT & ITEA 2 SYMPOSIUM
Our annual event is planned to take place at the end of October in Ghent, Belgium. After a sucessful event in Madrid in 2009, the focus will be put on the project exhibition where projects of ARTEMIS Call 1 and Call 2 will be displayed. For more information, check our website.
More information: www.artemisia-association.eu

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